

PHQAA

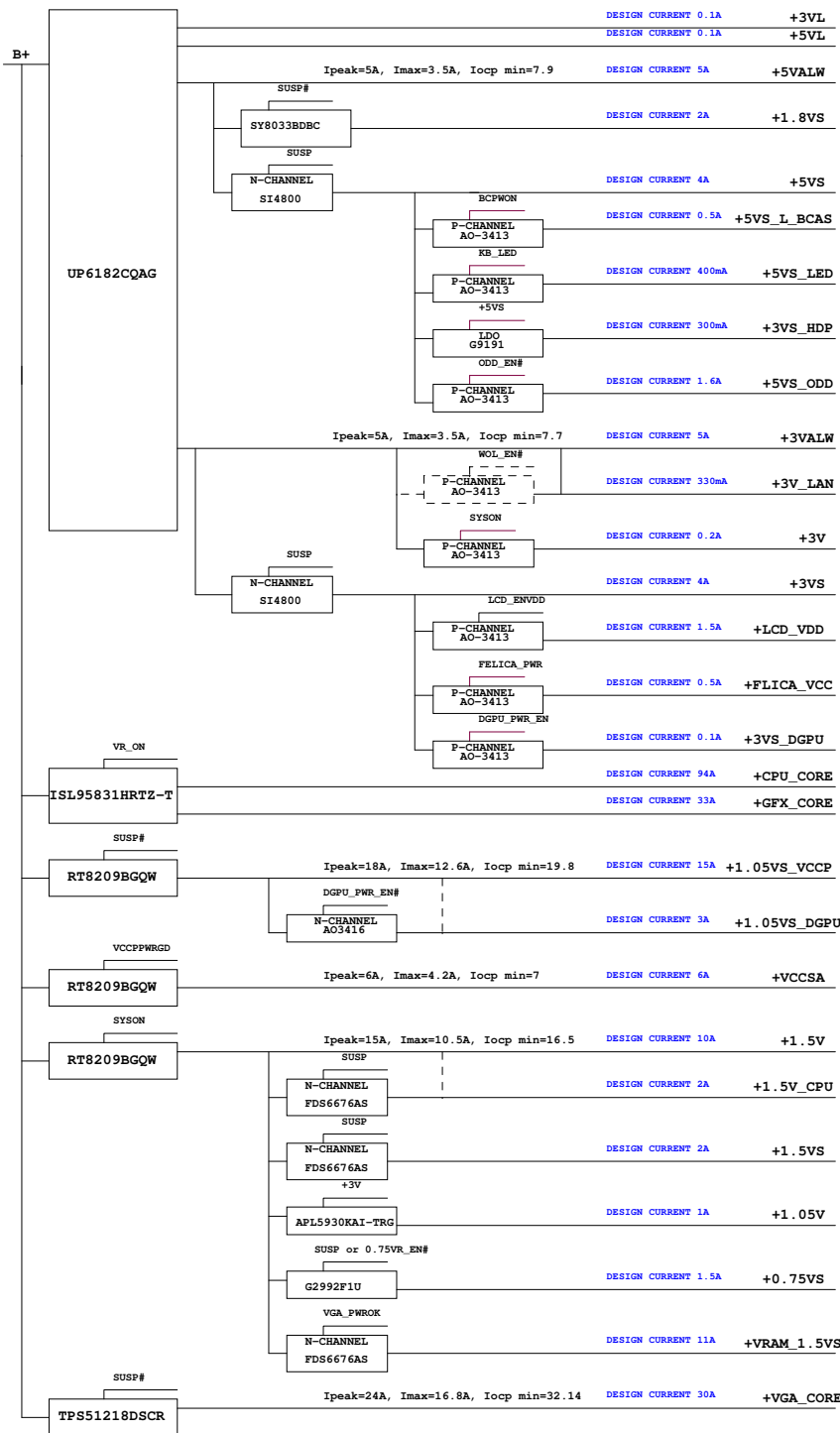
Marseille 10R/10RG

LA-6831P REV 0.3 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-07-05 Rev 0.1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number PHQAA LA-6831P M/B
				Date: Thursday, October 07, 2010	Rev 0.3
				Sheet 1	of 58





Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/08/03	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document Number	0.3
				PHQAA LA-6832P M/B	
				Date	Thursday, October 17, 2010
				Sheet	3 of 45

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA (OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

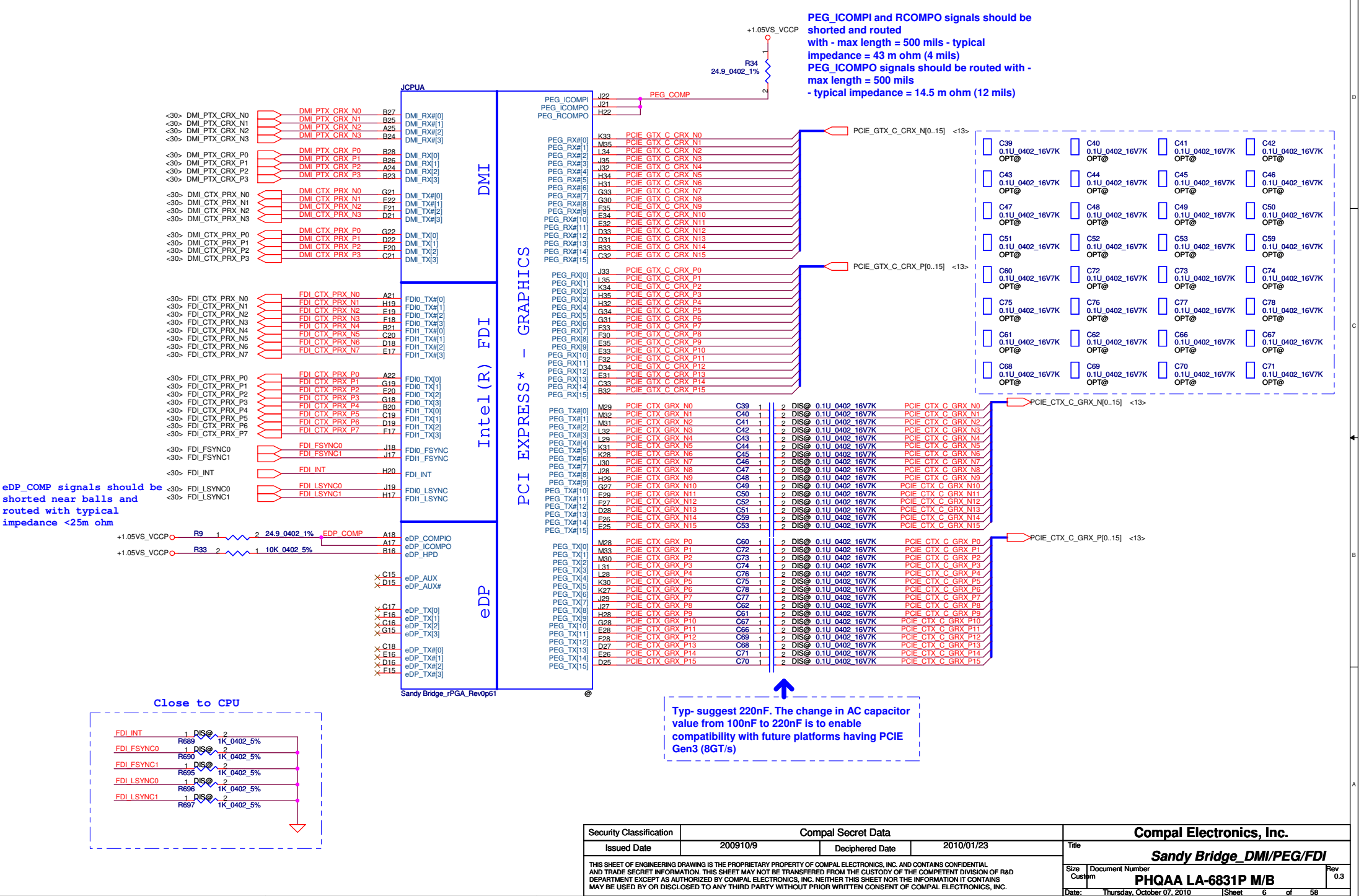
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	SPCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

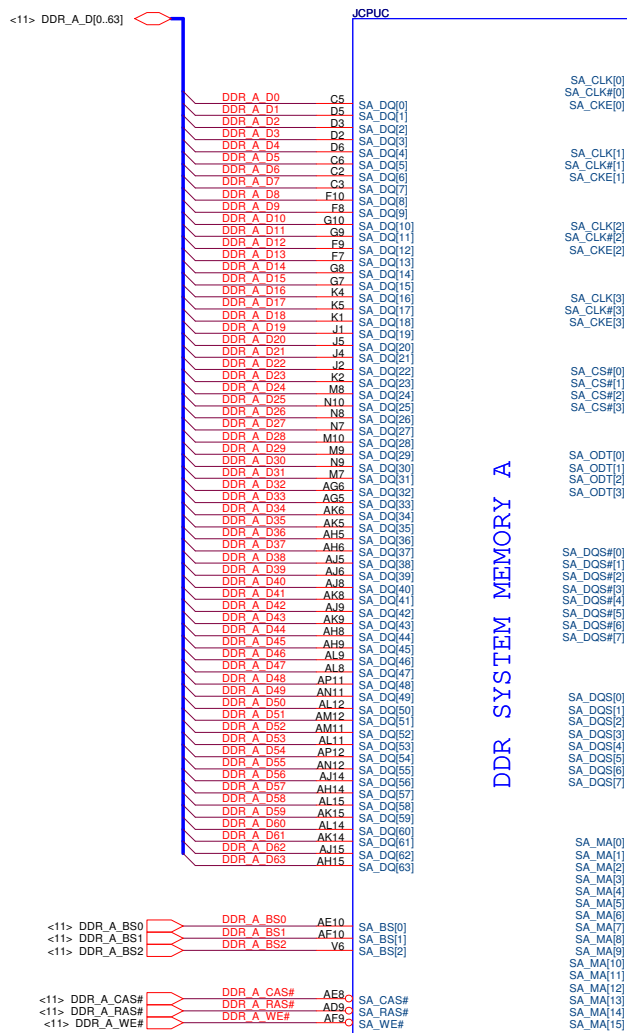
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

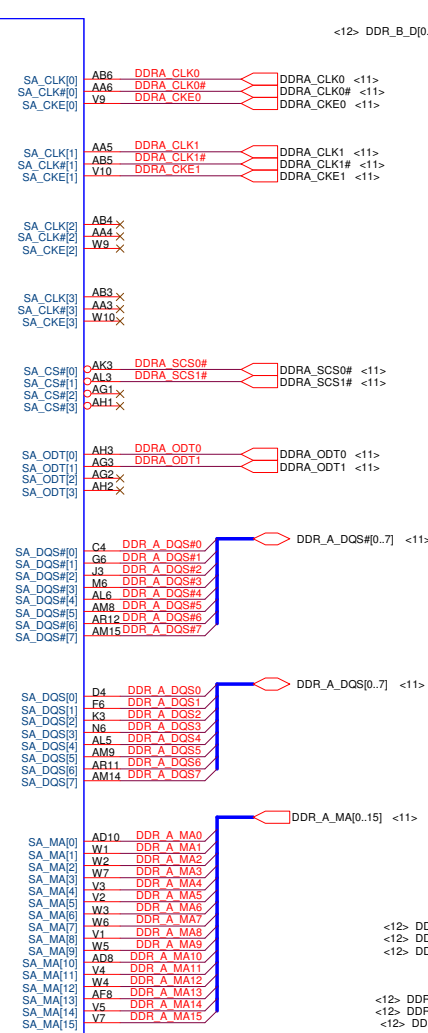
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	Notes List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number PHQAA LA-6831P M/B	Rev 0.3
				Date: Thursday, October 07, 2010	Sheet 4 of 58	



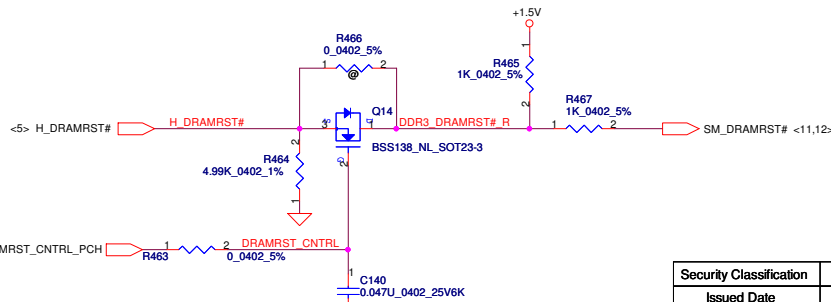
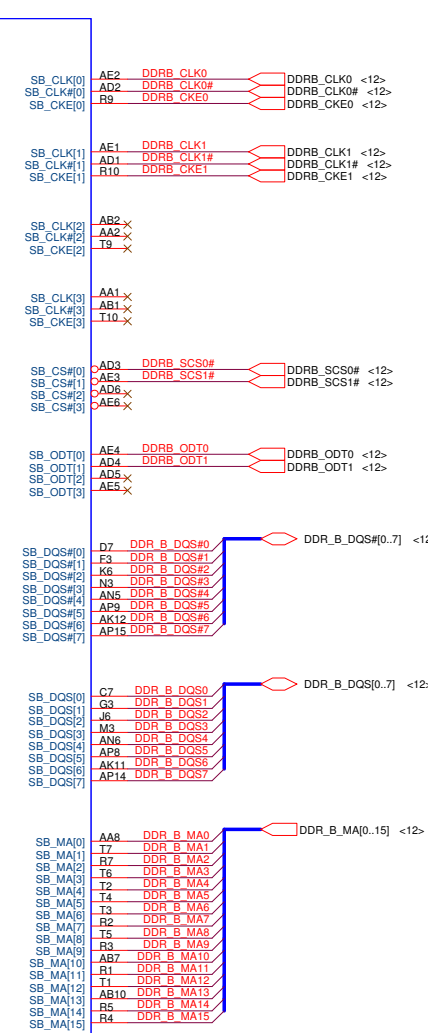
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	Sandy Bridge_DMI/PEG/FDI
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	PHQAA LA-6831P M/B
				Date	Thursday, October 07, 2010
				Sheet	6 of 58



DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Sandy Bridge_DDR3	
Size		Document Number		PHQAA LA-6831P M/B	
Date		Thursday, October 07, 2010		Sheet 7 of 58	

+CPU_CORE

JCPUF

POWER

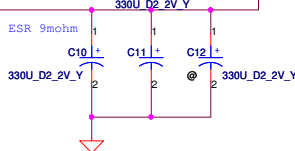
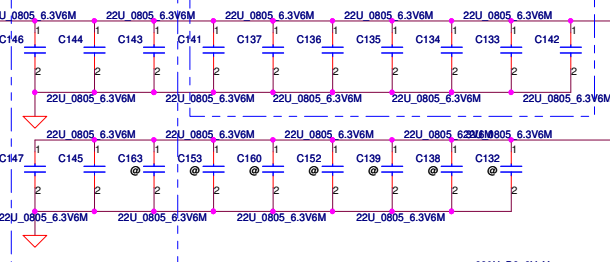
94A (Quad Core 45W)
53A (SV 35W)

8.5A

+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

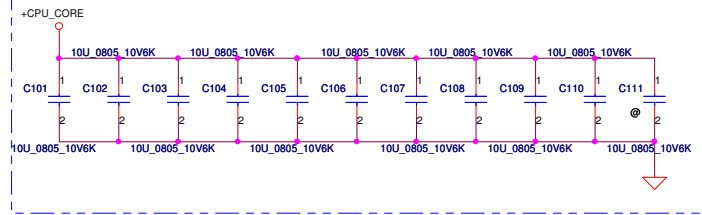
+1.05VS_VCCP

TOP Socket Cavity x 7

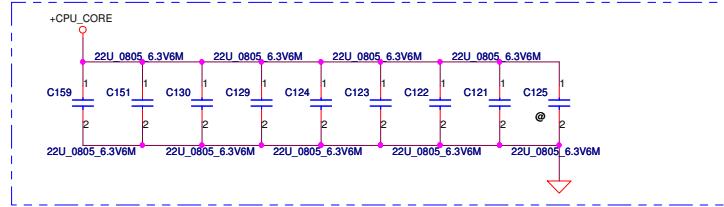


+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

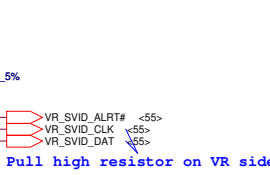
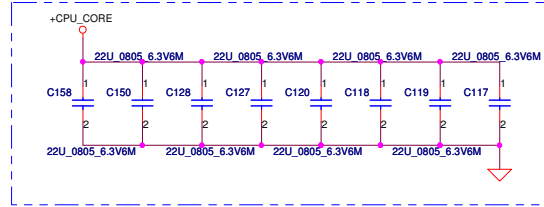
Bottom Socket Cavity



Top Socket Edge



Top Socket Cavity



Pull high resistor on VR side

+CPU_CORE

Close to CPU

VCC SENSE <55>
VSS SENSE <55>

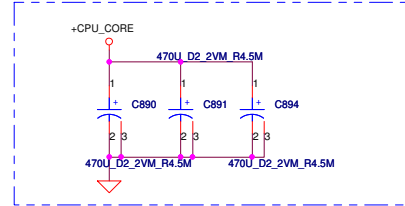
VCCIO SENSE <54>
VSSIO SENSE <54>

VCCIO SENSE <54>
VSSIO SENSE <54>

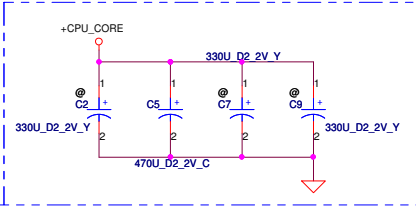
VCCIO SENSE <54>
VSSIO SENSE <54>

VCCIO SENSE <54>
VSSIO SENSE <54>

Co-Lay with C2, C5, C7, C9



Bottom Socket Edge



Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	200910/9	Title
	Deciphered Date	Sandy Bridge_POWER-1
	2010/01/23	Size
		Document Number
		PHQAA LA-6831P M/B
		Rev
		0.3
		Date
		Thursday, October 07, 2010
		Sheet
		8 of 58

ESR 17mohm

1

C873

330U_2.5V_M_R17

OPT@

2

Edge

Down Plan

JCPUG

SENSE
TENSES

1.8V RAIL

VREF

R3 -1.5V RAILS

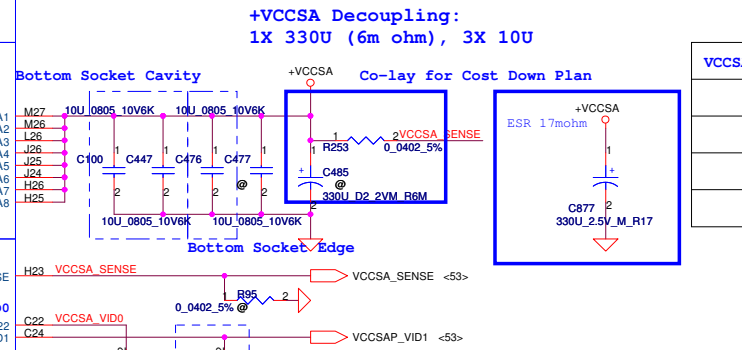
SA RAIL

MISC

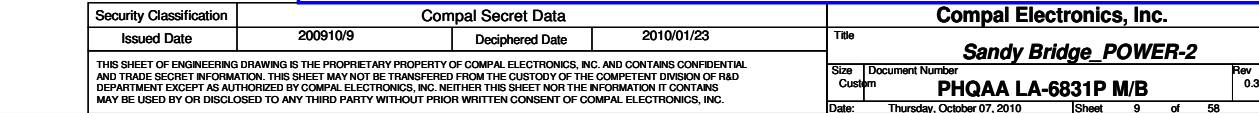
VCCPLL Decoupling:
1X 330U (6m ohm), 1X 10U, 2x1U

The diagram shows a top-down view of a PCB layout. A red power plane is labeled '+1.8VS' at the top left. A red microcontroller is located on the right side, with its VCCPLL pin connected to a red trace. The trace passes through a series of decoupling capacitors: a 330U capacitor (labeled '330U_B2_2.5VM_R15M'), a 10U capacitor (labeled '1U_0402_6.3V6K'), and two 1U capacitors (labeled '1U_0402_6.3V6K'). The capacitors are connected to a red ground plane at the bottom. The layout is labeled with various component values and part numbers, including 'R76', 'C185', 'C186', 'C206', and 'C230'. The text 'VCCPLL Decoupling: 1X 330U (6m ohm), 1X 10U, 2x1U' is written in blue at the top.

WWW.AliSaler.Com

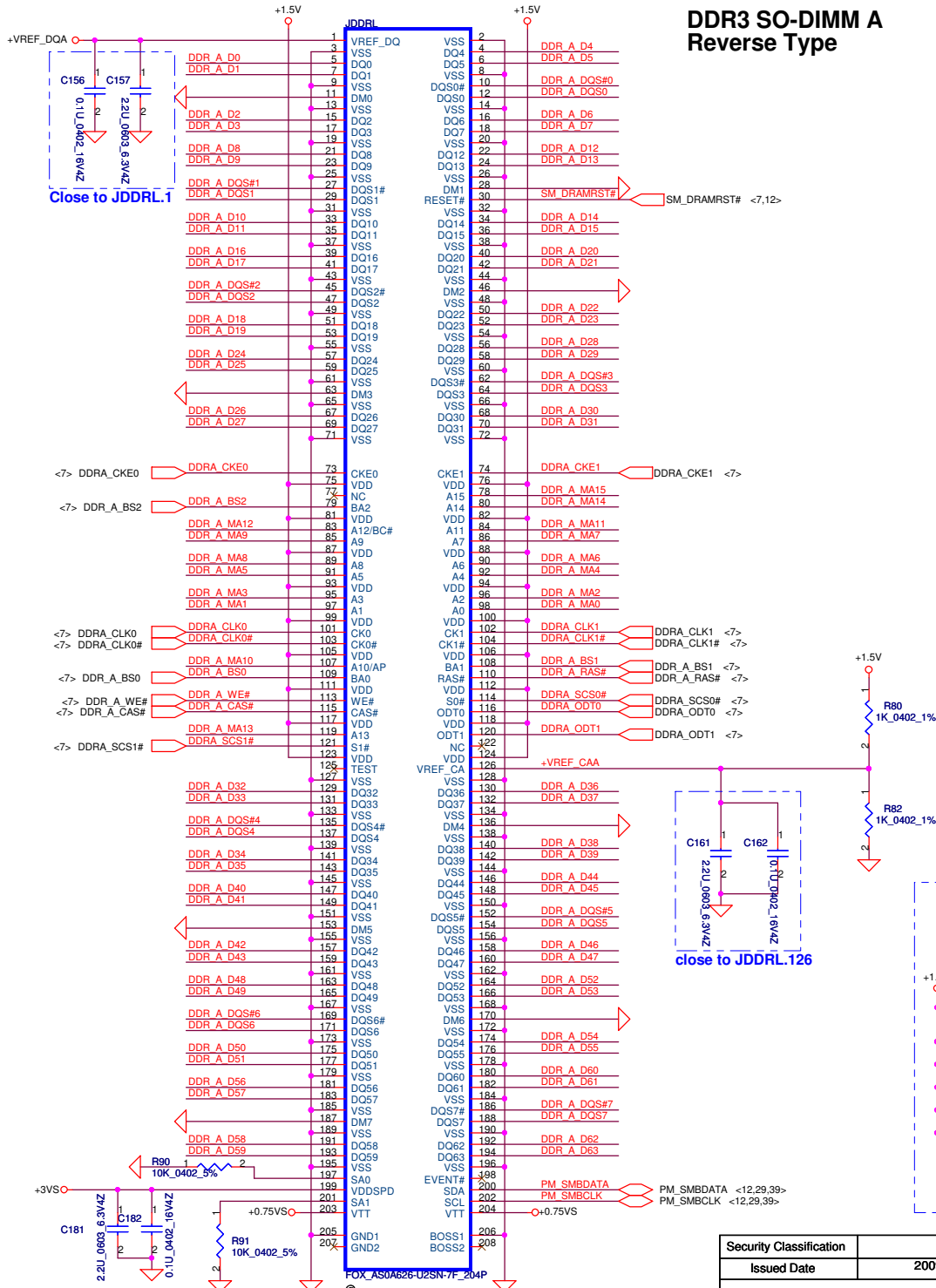


For Sandy Bridge

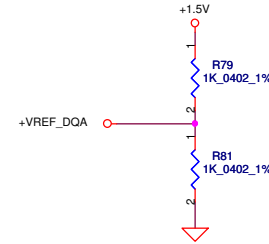




DDR3 SO-DIMM A Reverse Type



DDR_A_DQS[0..7] <7>
 DDR_A_DQS# [0..7] <7>
 DDR_A_D[0..63] <7>
 DDR_A_MA[0..15] <7>

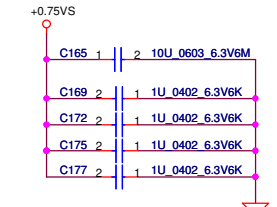
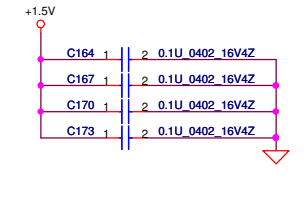
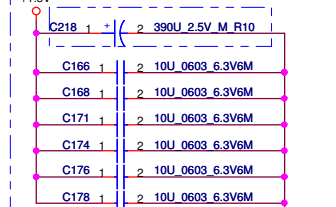


Layout Note:
Place near JDDR.L

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

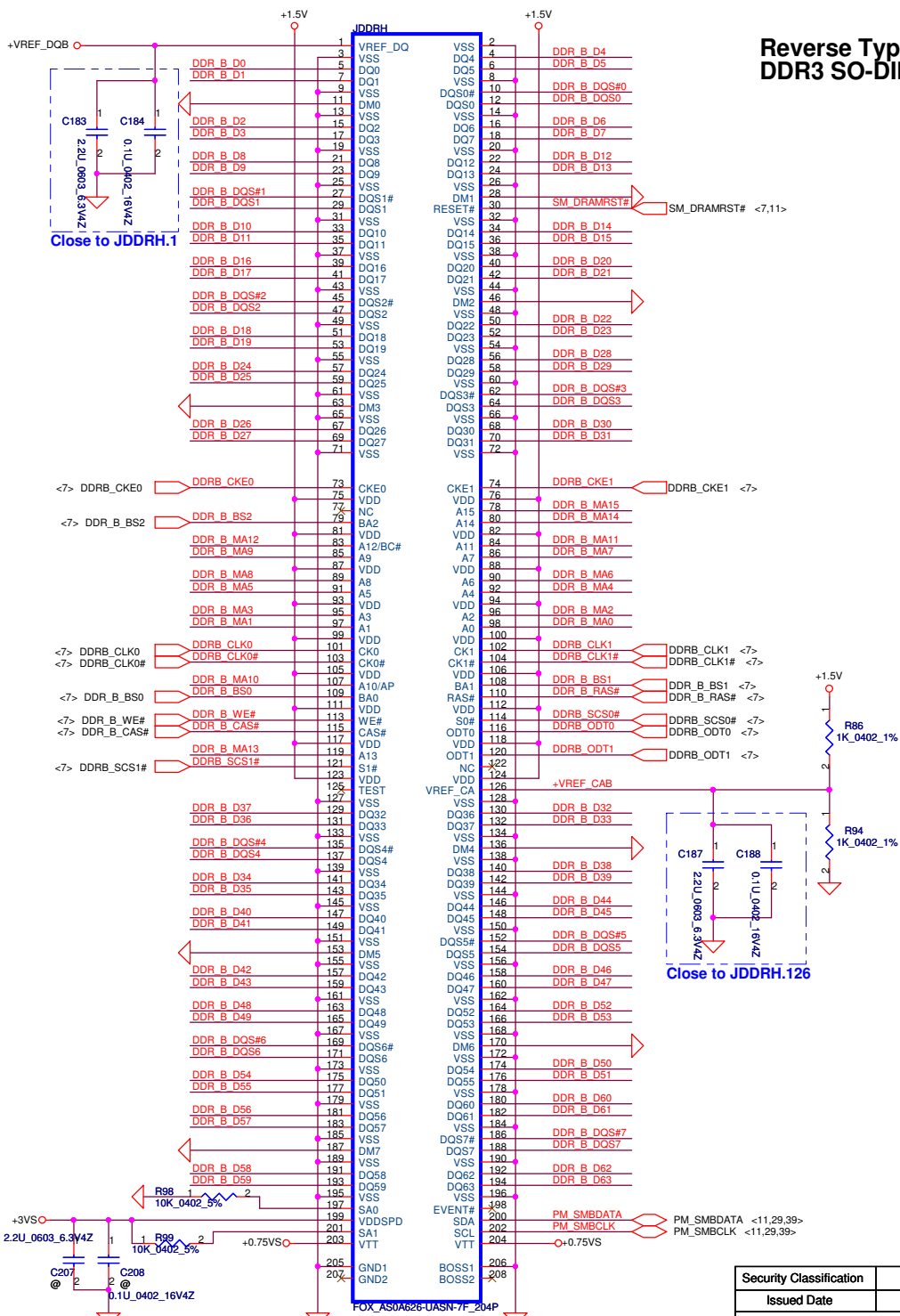
Layout Note: Place near JDDR.L203 and 204

Change C218 to OSCON at DVT

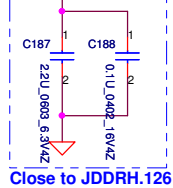
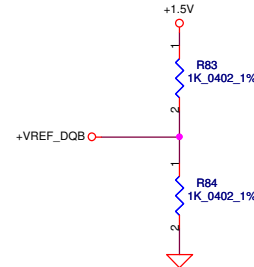


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DDR.III-SODIMMO	
Size	Document Number	Customer	Rev	PHQAA LA-6831P M/B	
Date:	Thursday, October 07, 2010	Sheet	11	of 58	

Reverse Type DDR3 SO-DIMM B



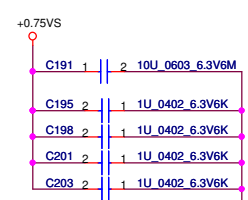
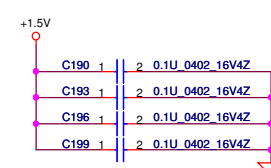
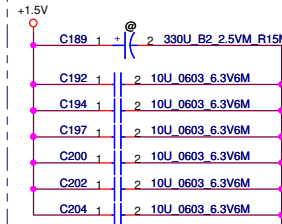
- DDR_B_DQS#[0..7] <7>
- DDR_B_DQS[0..7] <7>
- DDR_B_D[0..63] <7>
- DDR_B_MA[0..15] <7>



Layout Note:
Place near JDDR.H

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDR.H.203 and 204



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title DDR3II-SODIMM1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 0.3
				PHQAA LA-6831P M/B	
				Date: Thursday, October 07, 2010	Sheet 12 of 58



Mode	VID1	VID0	+VGA_CORE
P0 (Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

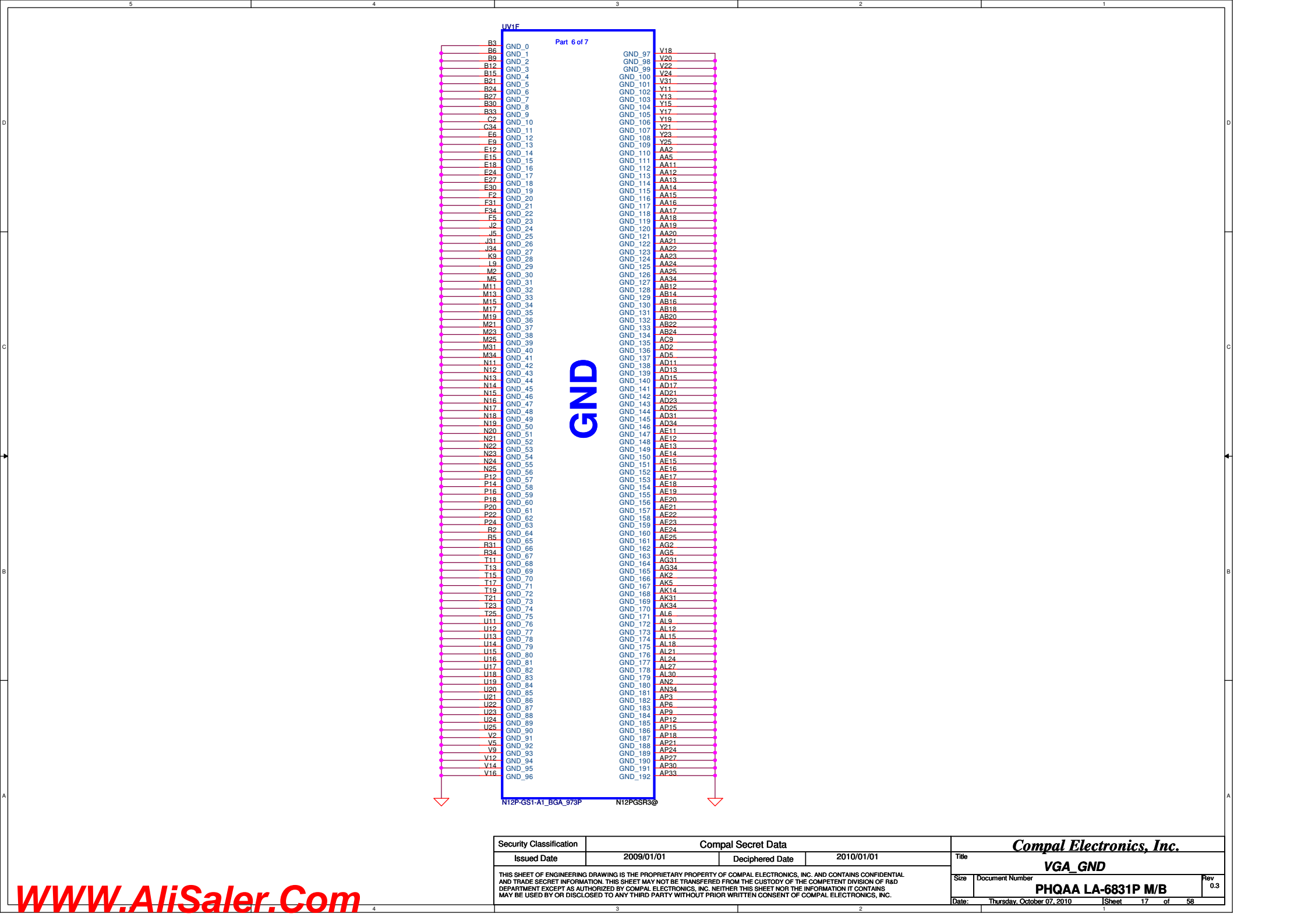
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD



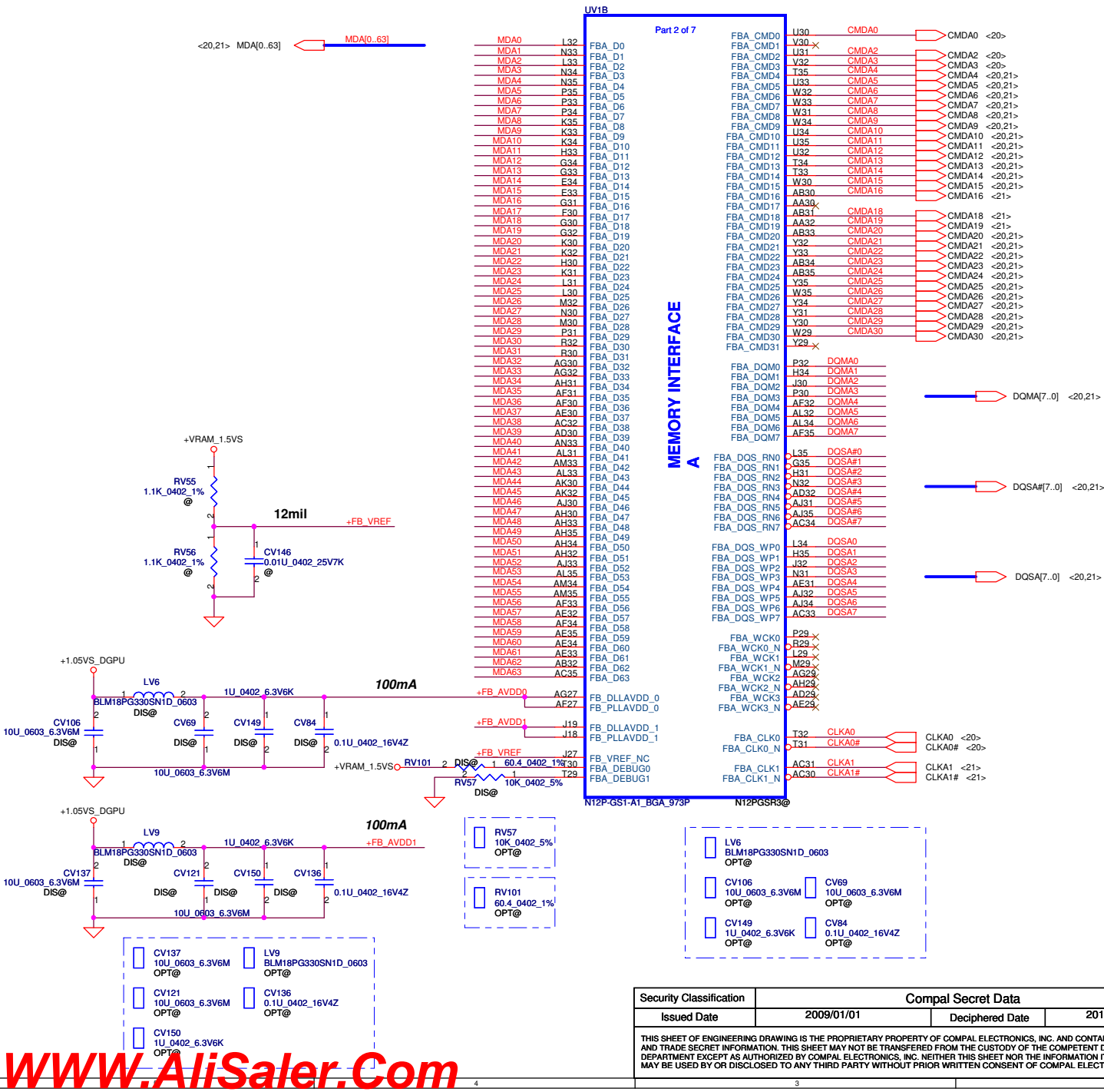
The diagrams illustrate the decoupling network for the N11P-GE1 and N11M-OP1 modules. The top diagram shows the power supply input stage, the middle diagram shows the +VGA_CORE supply rail decoupling, and the bottom diagram shows the +VGA_CORE supply rail decoupling.

- | | | | | | | |
|---|------------|--------------------|------------|--|---|-----|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc.
VGA_VGA CORE | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 | | | |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. | | | | Title | | |
| | | | | Size | Document Number | Rev |
| | | | | | PHQAA LA-6831P M/B
Date: Thursday, October 07, 2010 Sheet 15 of 58 | |

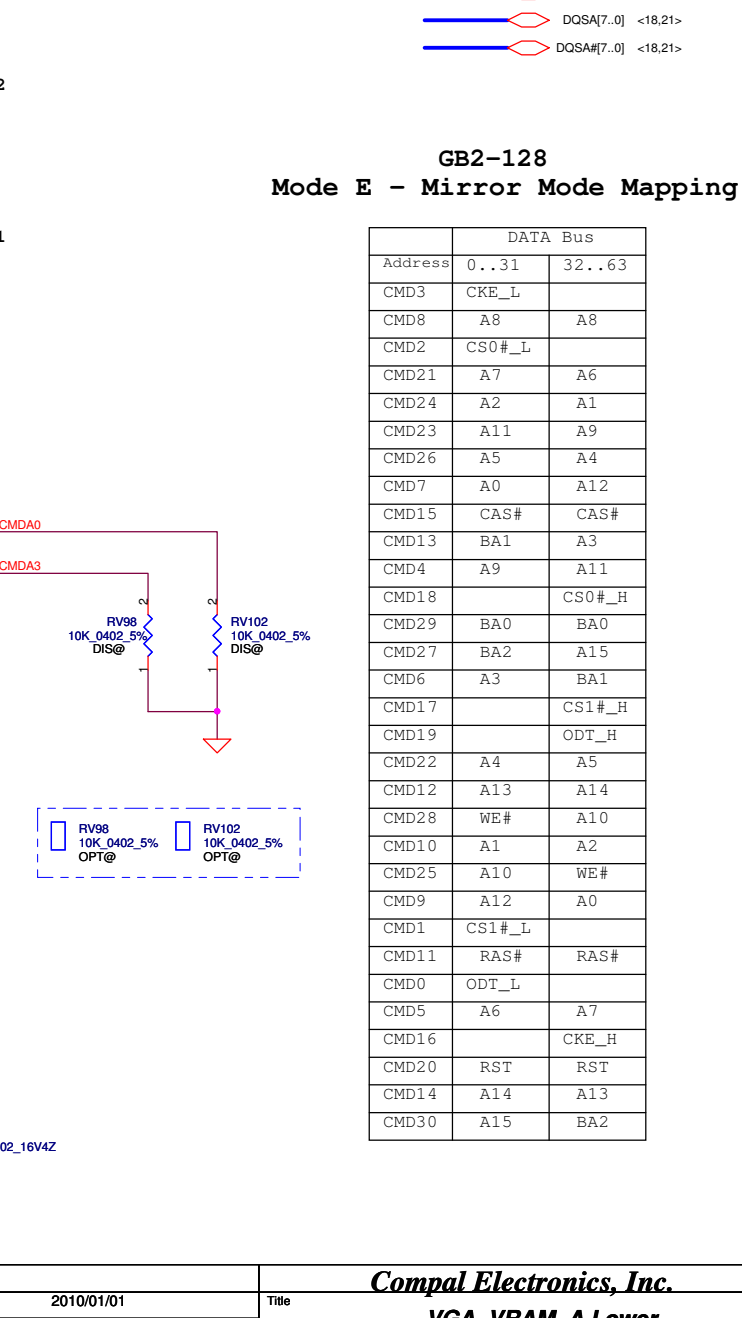
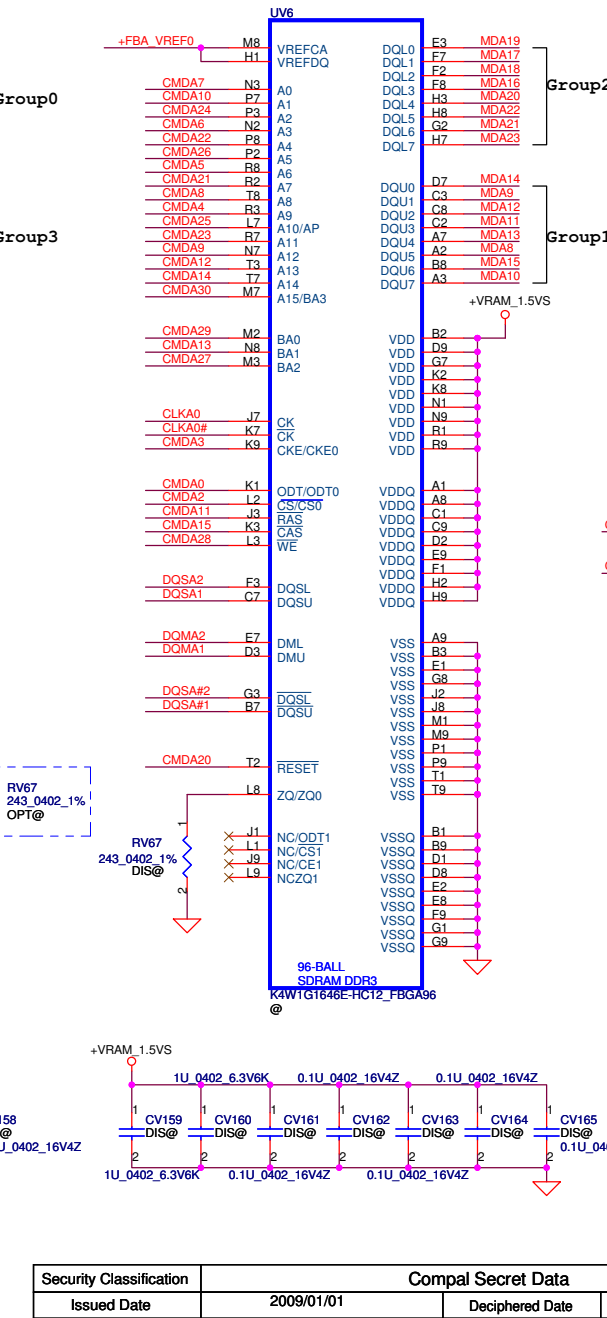
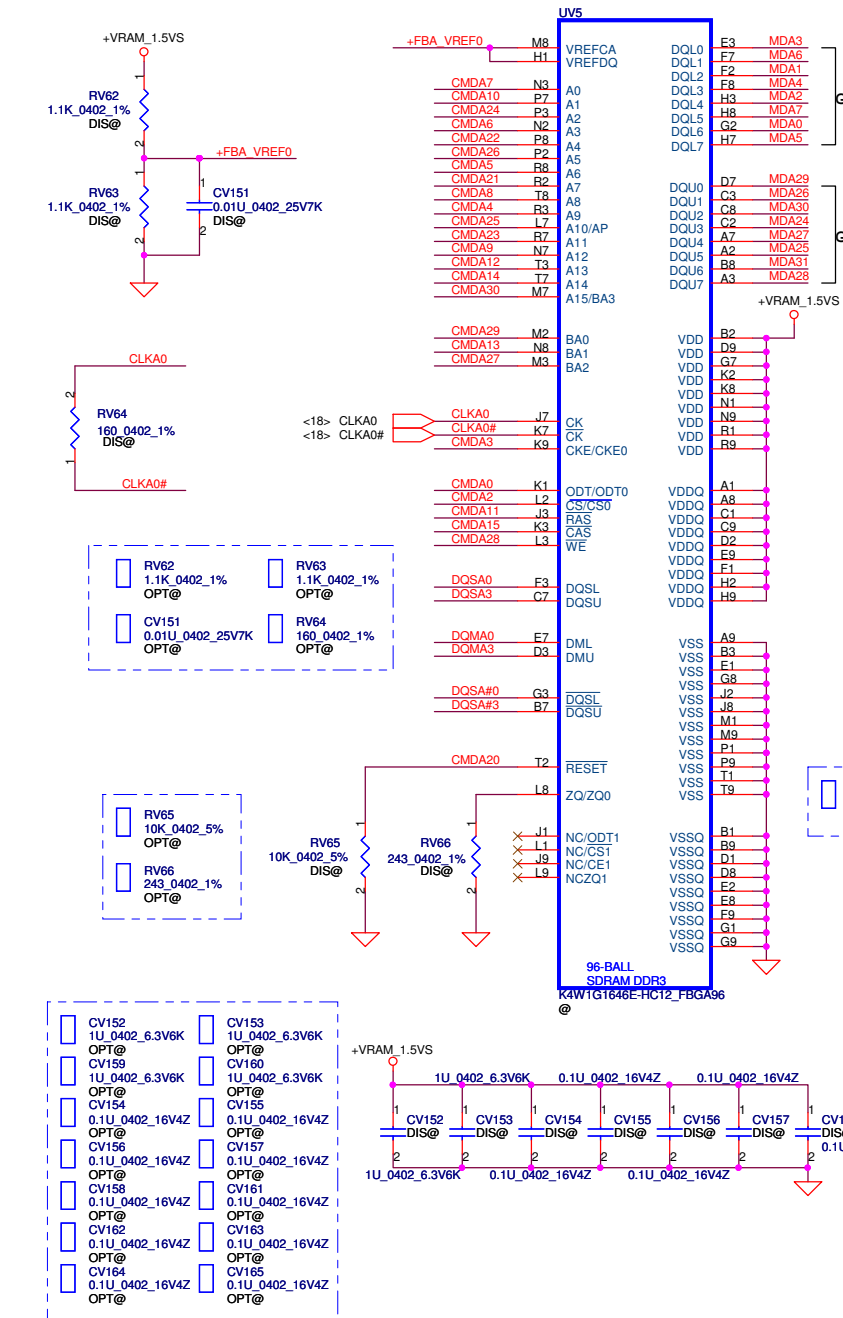


GB2-128
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



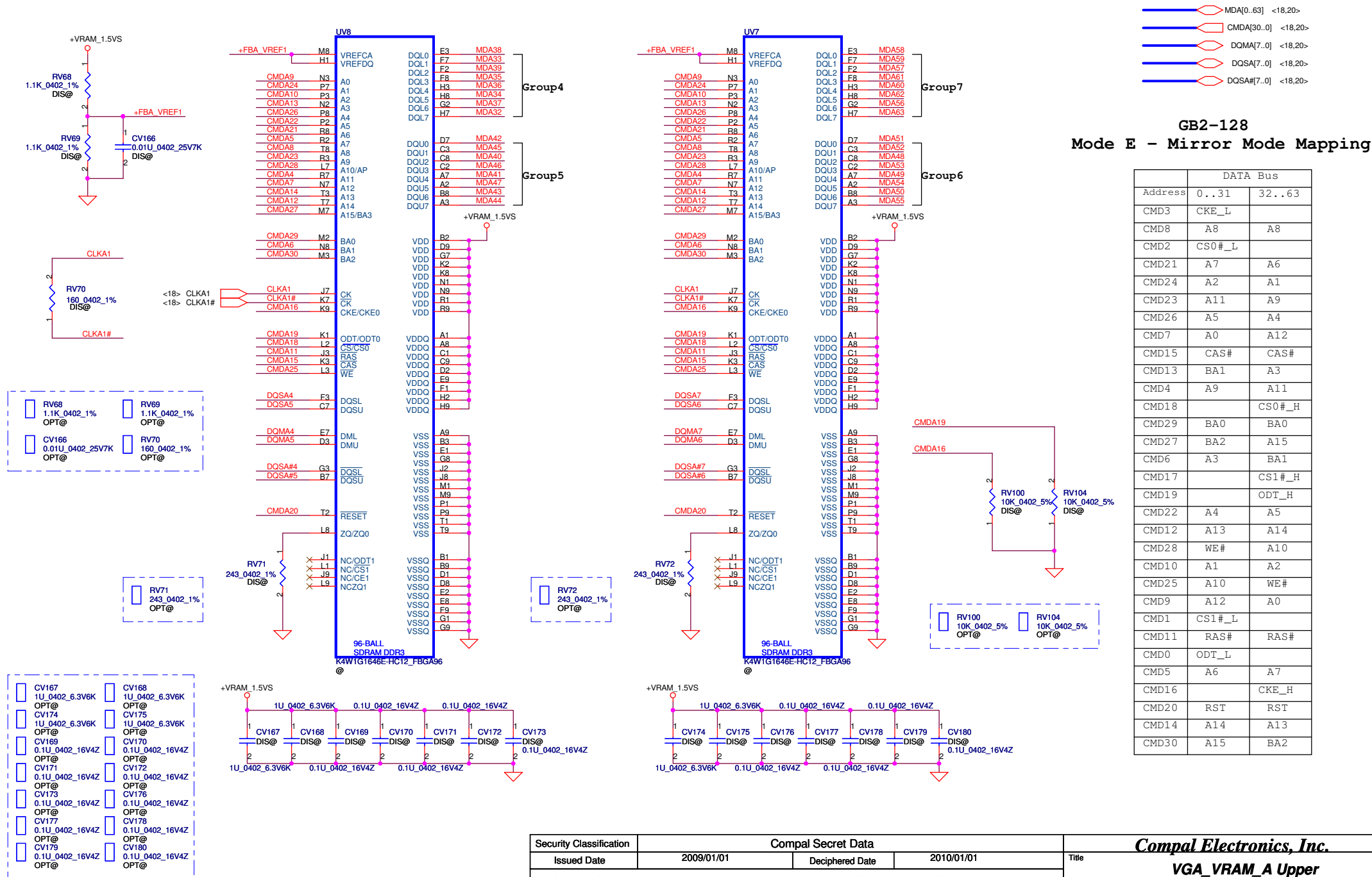
Memory Partition A - Lower 32 bits



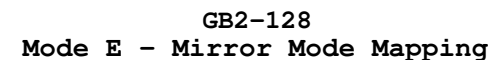
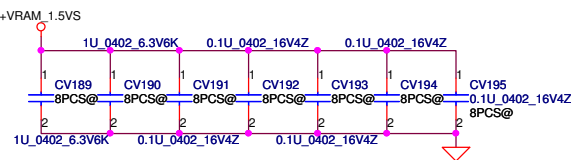
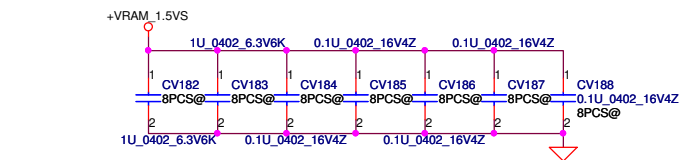
DATA Bus	
Address	0..31 32..63
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

GB2-128
Mode E - Mirror Mode Mapping

Memory Partition A - Upper 32 bits



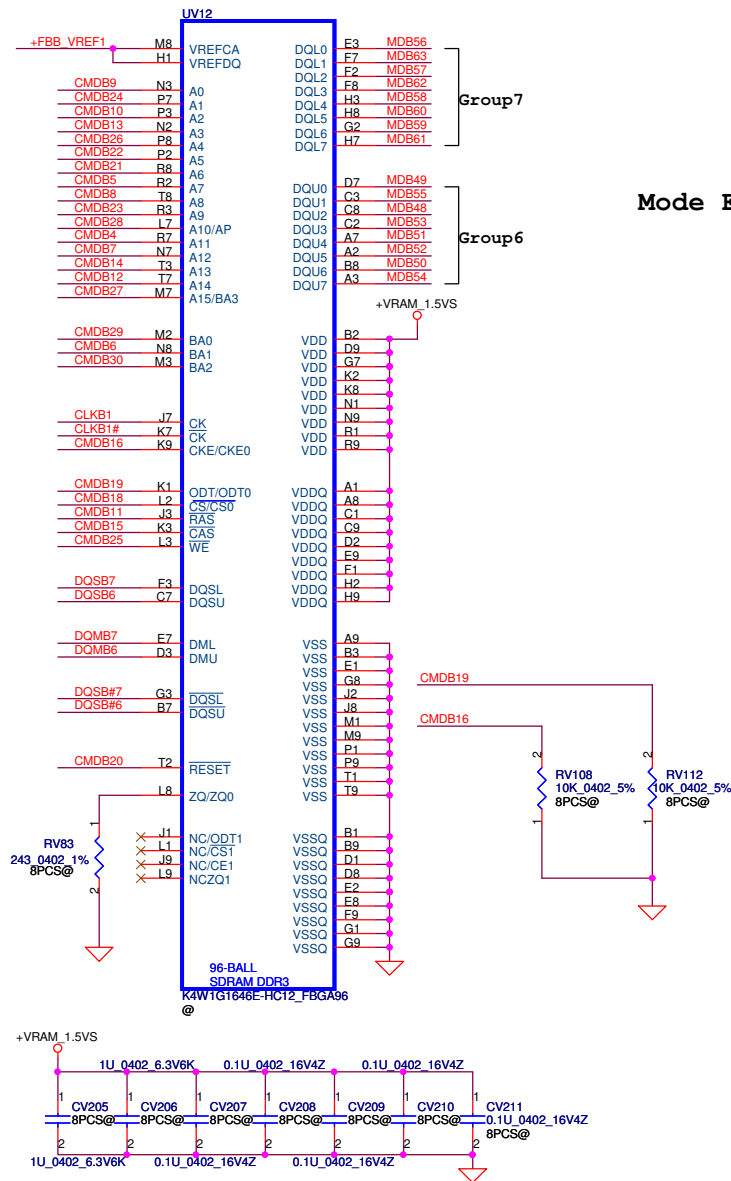
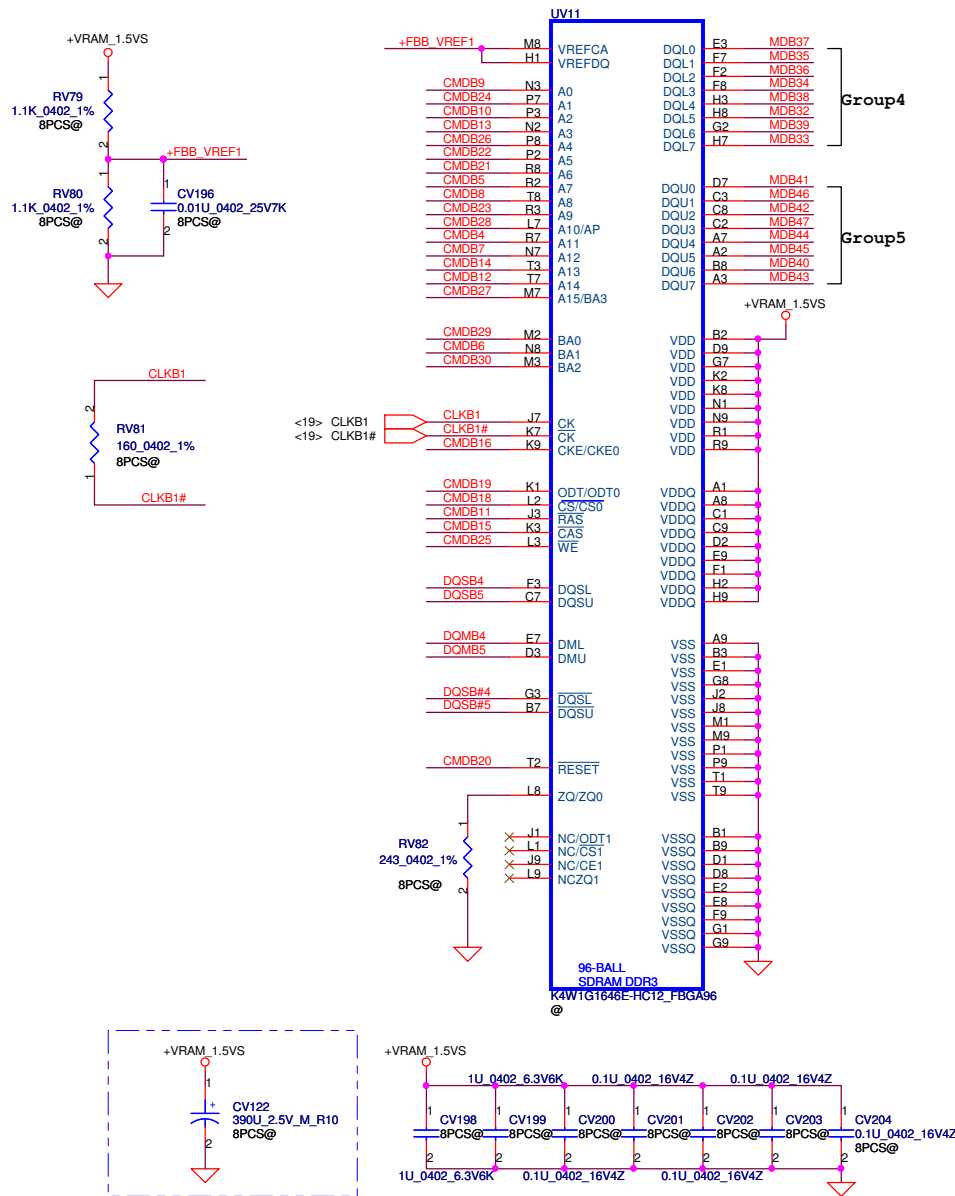
WWW.AliSaler.Com



	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2009/01/01	Deciphered Date	2010/01/01				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	VGA_VRAM_C Lower		
				Size Custom	Document Number	PHQAA LA-6831P M/B	Rev 0.3
				Date:	Thursday, October 07, 2010	Sheet 22 of 58	

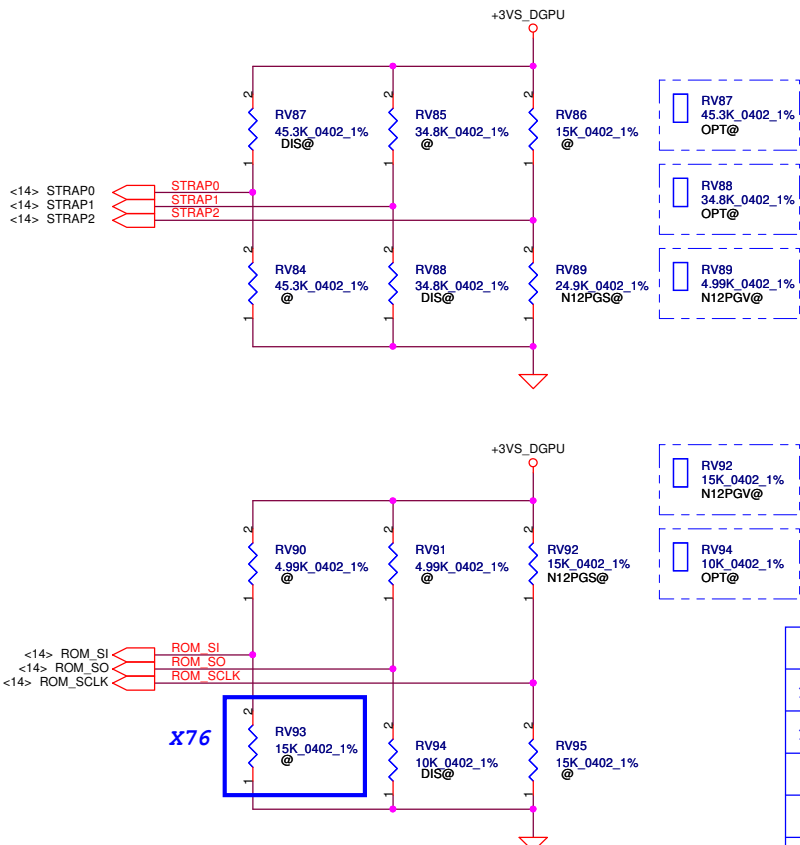
Memory Partition C - Upper 32 bits



GB2-128 Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	VGA_VRAM_C Upper	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				PHQAA LA-6831P M/B	
				Date: Thursday, October 07, 2010	Rev 0.3
				Sheet 23 of 58	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x1050	Pull up 15K	Pull down 5K

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

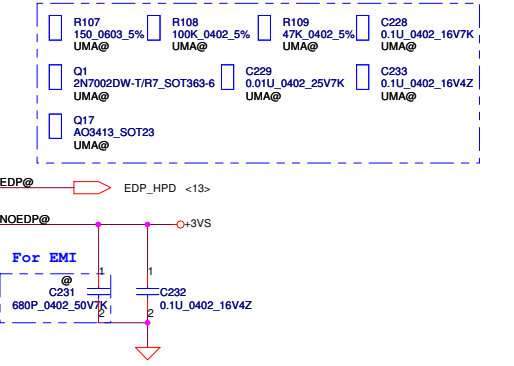
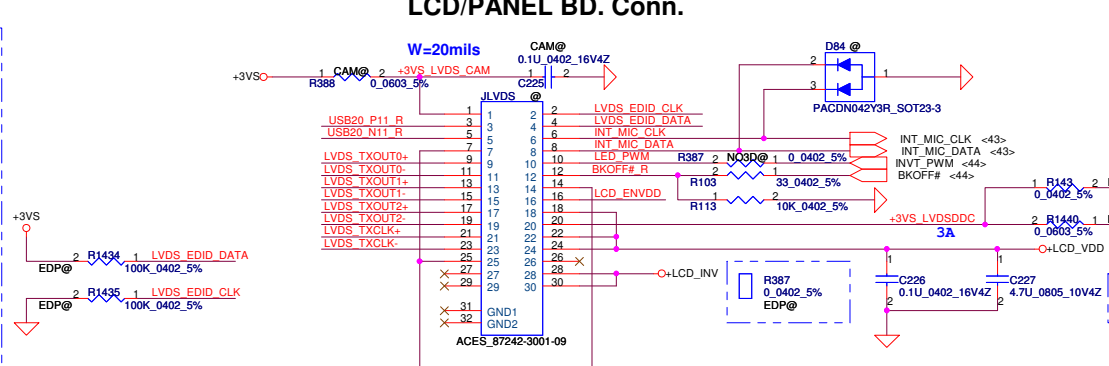
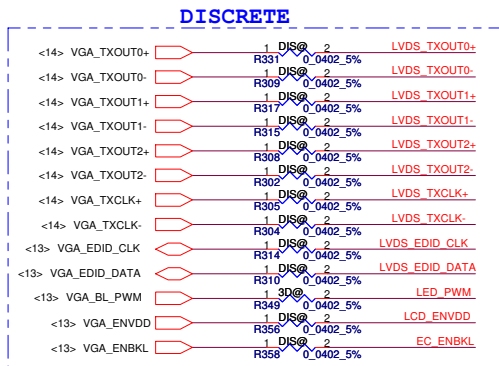
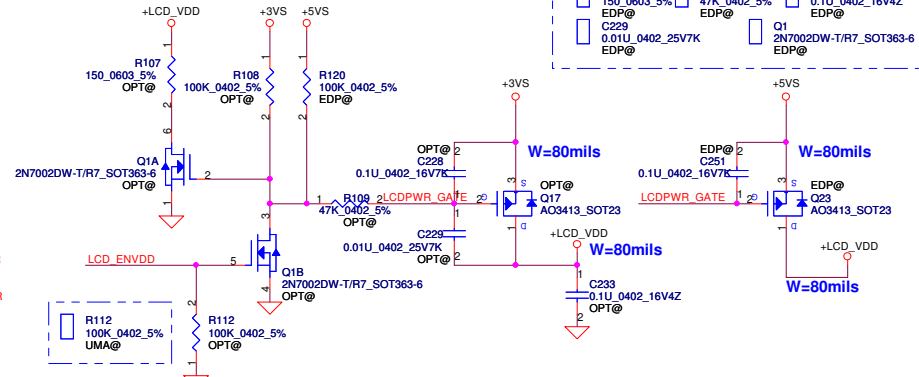
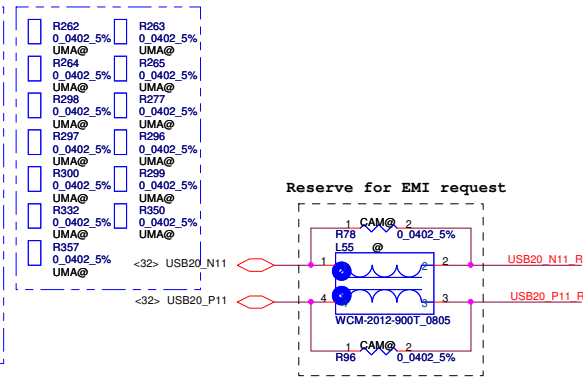
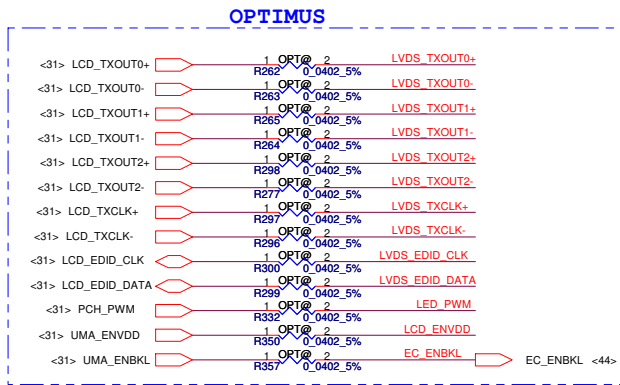
SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

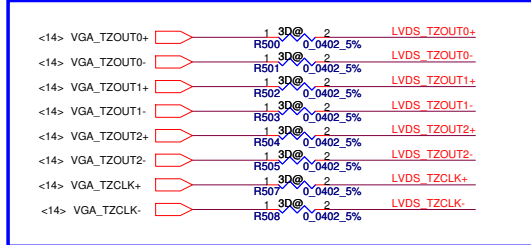
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k (SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	512MB	0011	PD 20K (SD034200280)
	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K (SD034453280)

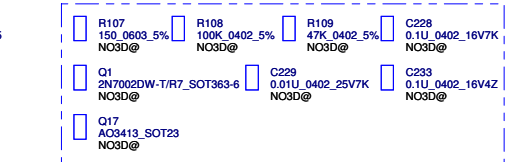
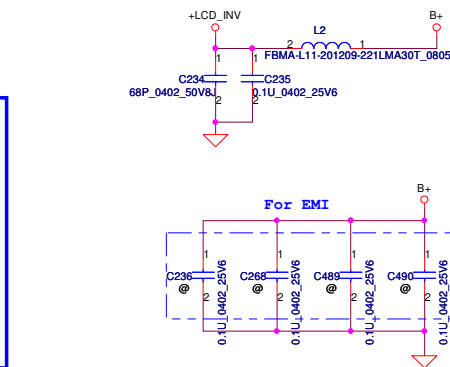
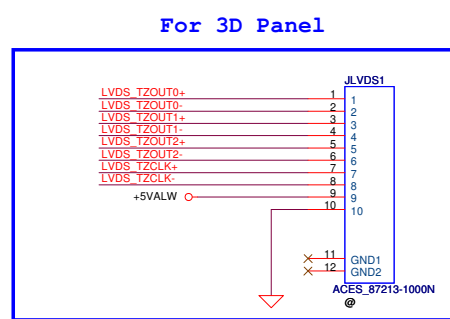
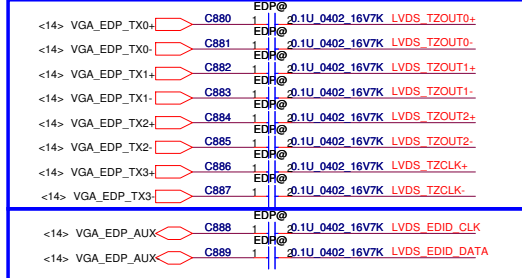
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				PHQAA LA-6831P M/B	
				Date: Thursday, October 07, 2010	Sheet 24 of 58



DISCRETE for Full-HD and 3D LVDS Panel



DISCRETE for Full-HD and 3D eDP Panel



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	LVDS/eDP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number PHQAA LA-6831P M/B
				Date	Thursday, October 07, 2010
				Sheet	25 of 58

OPTIMUS

<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

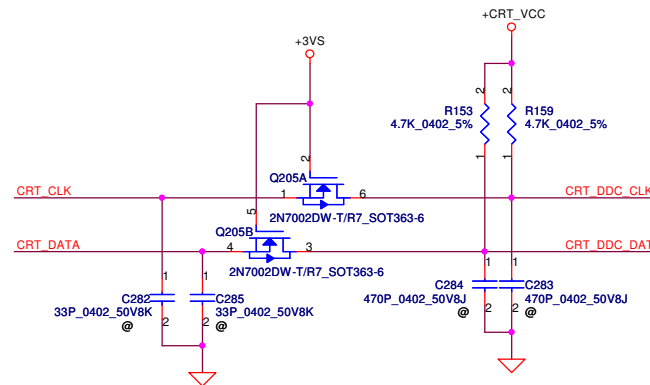
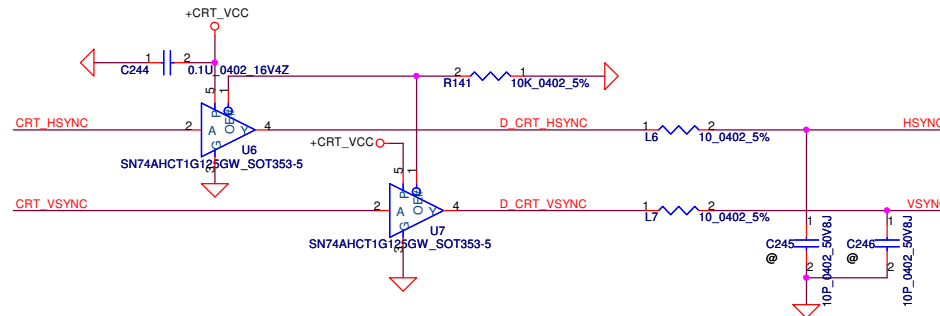
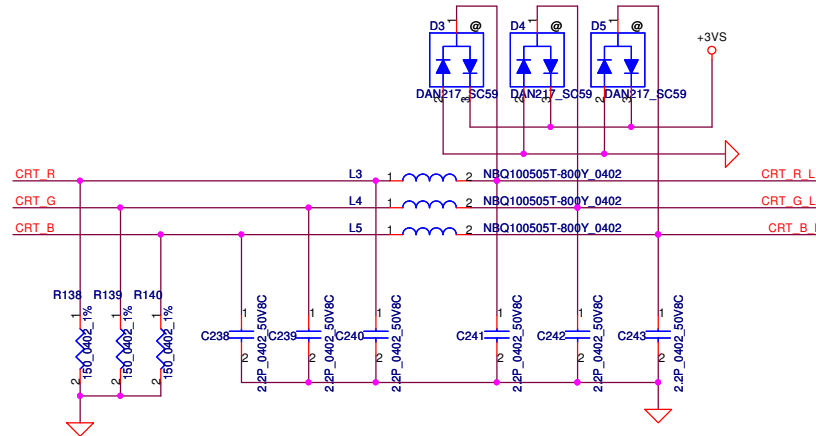
Close to CRT Connector

R200 0.0402_5% UMA@	R204 0.0402_5% UMA@	R211 0.0402_5% UMA@
R213 0.0402_5% UMA@	R235 0.0402_5% UMA@	R236 0.0402_5% UMA@
R261 0.0402_5% UMA@		

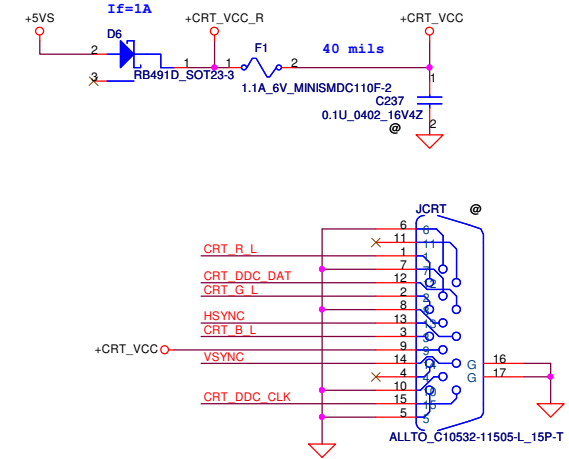
DISCRETE

<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector

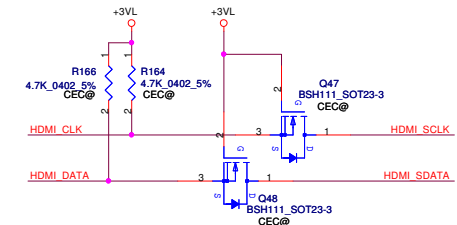
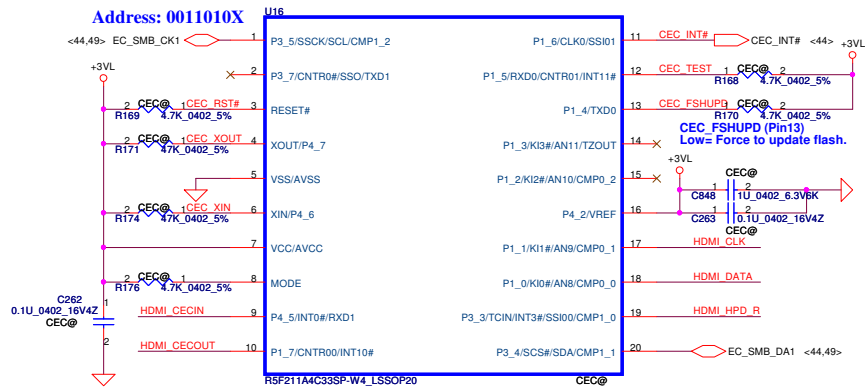
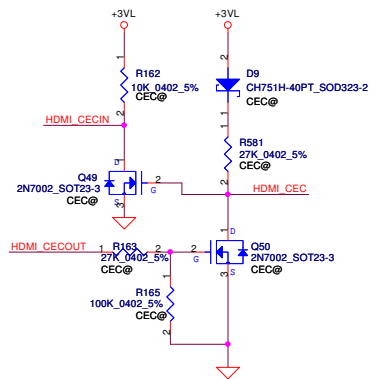


CRT CONNECTOR











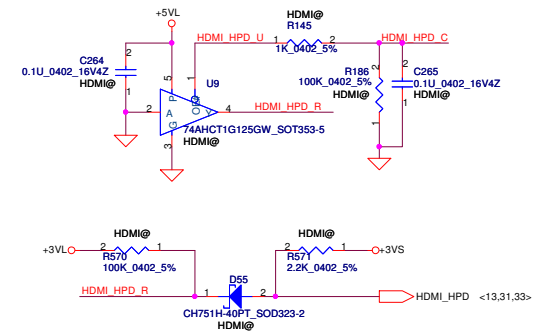
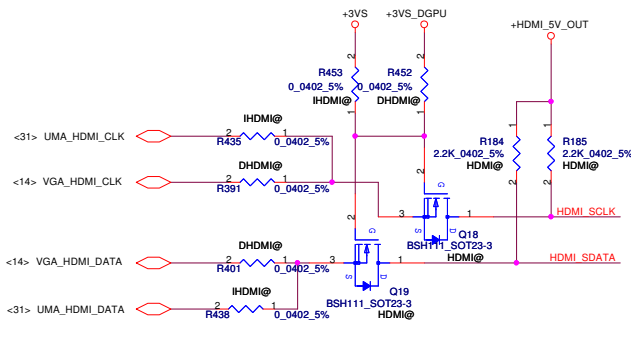
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	CRT
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					PHQAA LA-6831P M/B
				Date	Thursday, October 07, 2010
				Sheet	26 of 58

HDMI CEC Controller



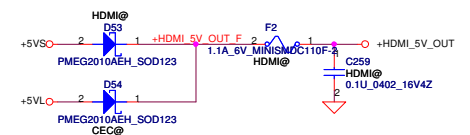
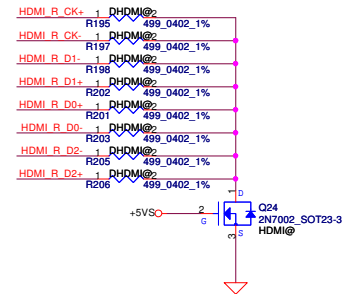
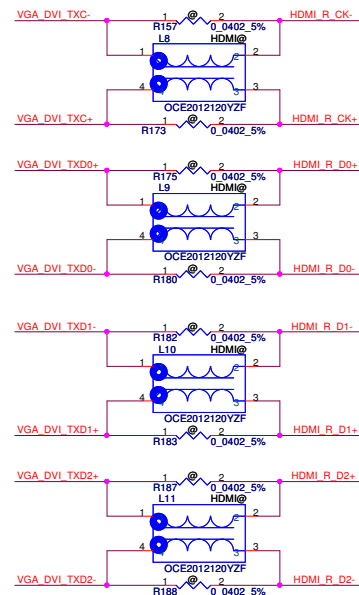
For DISCRETE

<14>	VGA_HDMI_CLK+		CV296	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXC+
<14>	VGA_HDMI_CLK-		CV293	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXC-
<14>	VGA_HDMI_TX0+		CV294	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXD0+
<14>	VGA_HDMI_TX0-		CV297	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXD0-
<14>	VGA_HDMI_TX1+		CV299	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXD1+
<14>	VGA_HDMI_TX1-		CV298	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXD1-
<14>	VGA_HDMI_TX2+		CV295	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXD2+
<14>	VGA_HDMI_TX2-		CV300	1	2	0.1U_0402_16V7K_DHDM1@	VGA_DVI_TXD2-

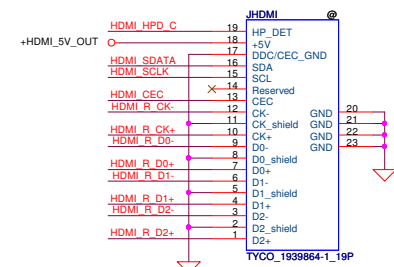


For Optimus

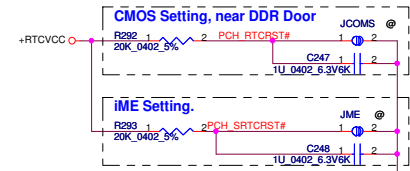
Address	Disassembly	Comment
<31> UMA_HDMI_TXC+	CV308 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC+
<31> UMA_HDMI_TXC-	CV304 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC-
<31> UMA_HDMI_TX0+	CV306 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0+
<31> UMA_HDMI_TX0-	CV302 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0-
<31> UMA_HDMI_TX1+	CV303 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1+
<31> UMA_HDMI_TX1-	CV301 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1-
<31> UMA_HDMI_TX2+	CV307 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2+
<31> UMA_HDMI_TX2-	CV305 1 2 0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2-



HDMI Connector

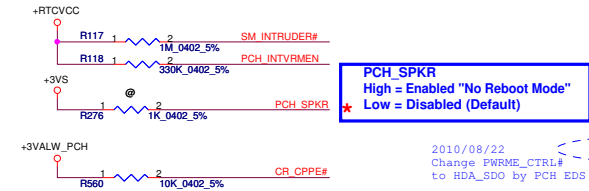


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	200910/9	Deciphered Date	2010/01/23	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI Conn./CEC		
				Size	Document Number	Rev
				PHQAA LA-6831P M/B		0.3
				Date:	Thursday, October 07, 2010	Sheet 27 of 58



Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)



HDA_SDO

ME debug mode, this signal has a weak internal pull down

★Low = Disable (default)

High = Enable (flash descriptor security override)

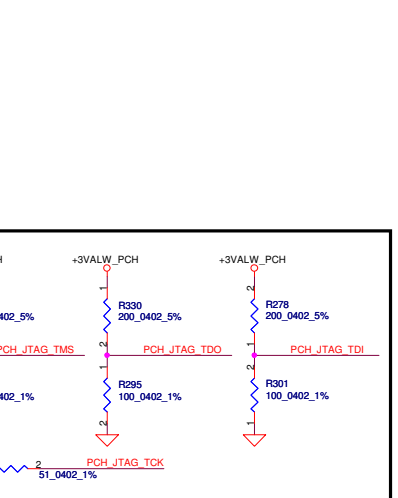
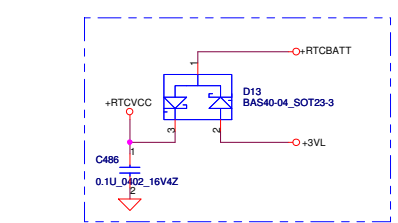
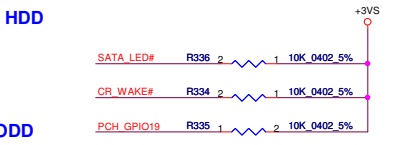
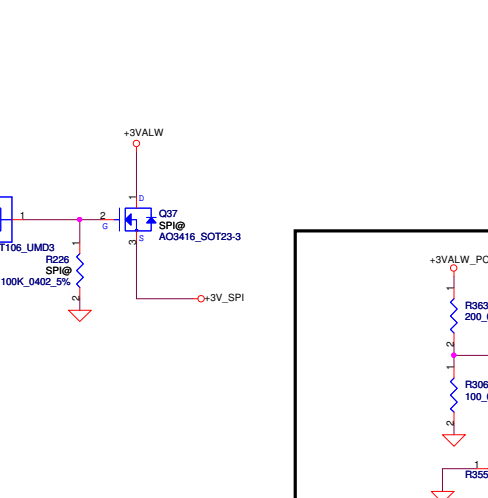
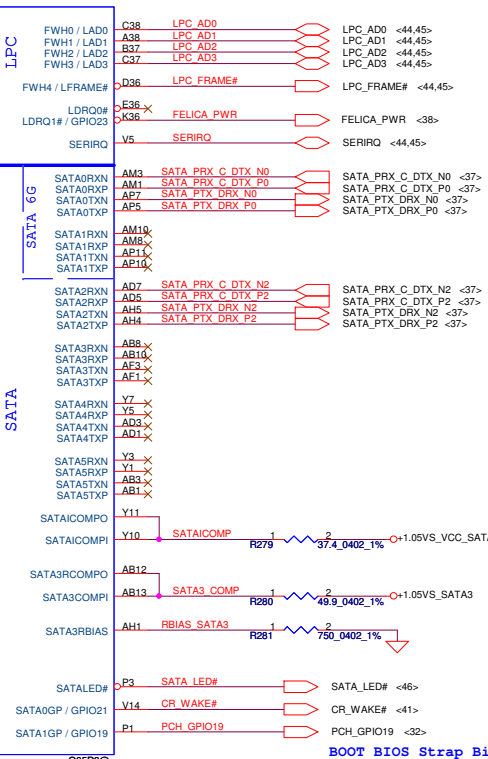
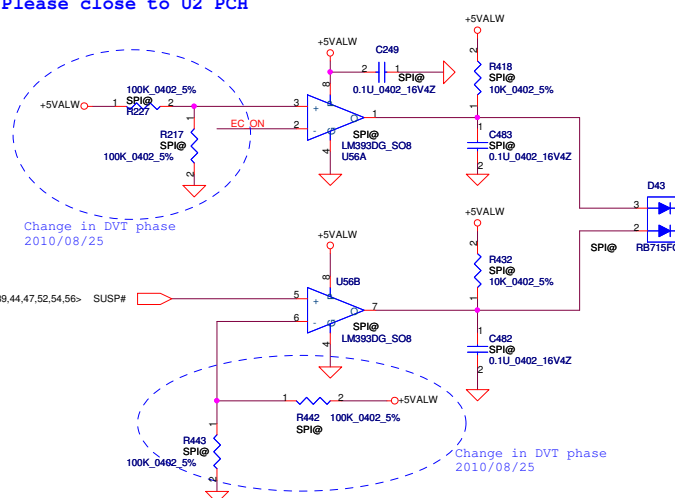
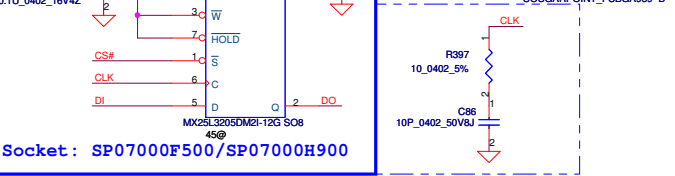
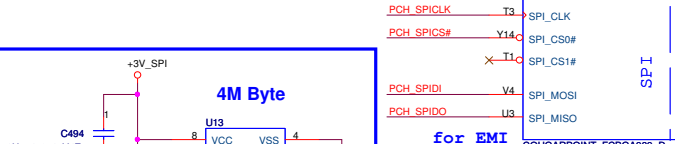
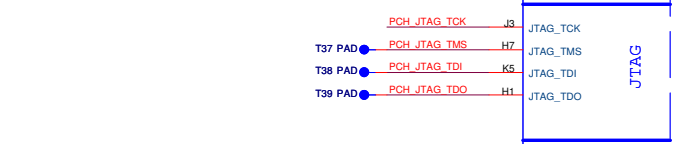
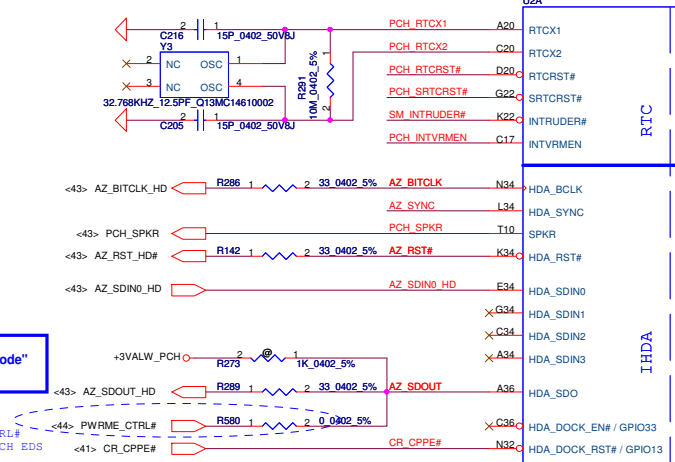
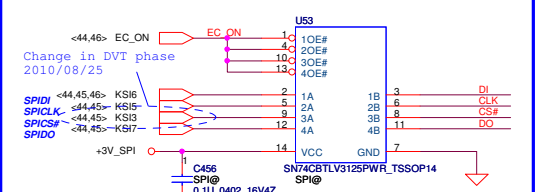
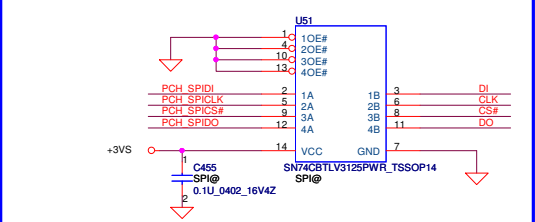
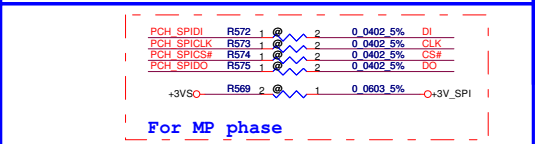
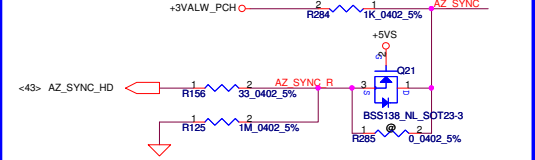
HDA_SYNC

★This signal has a weak internal pull down

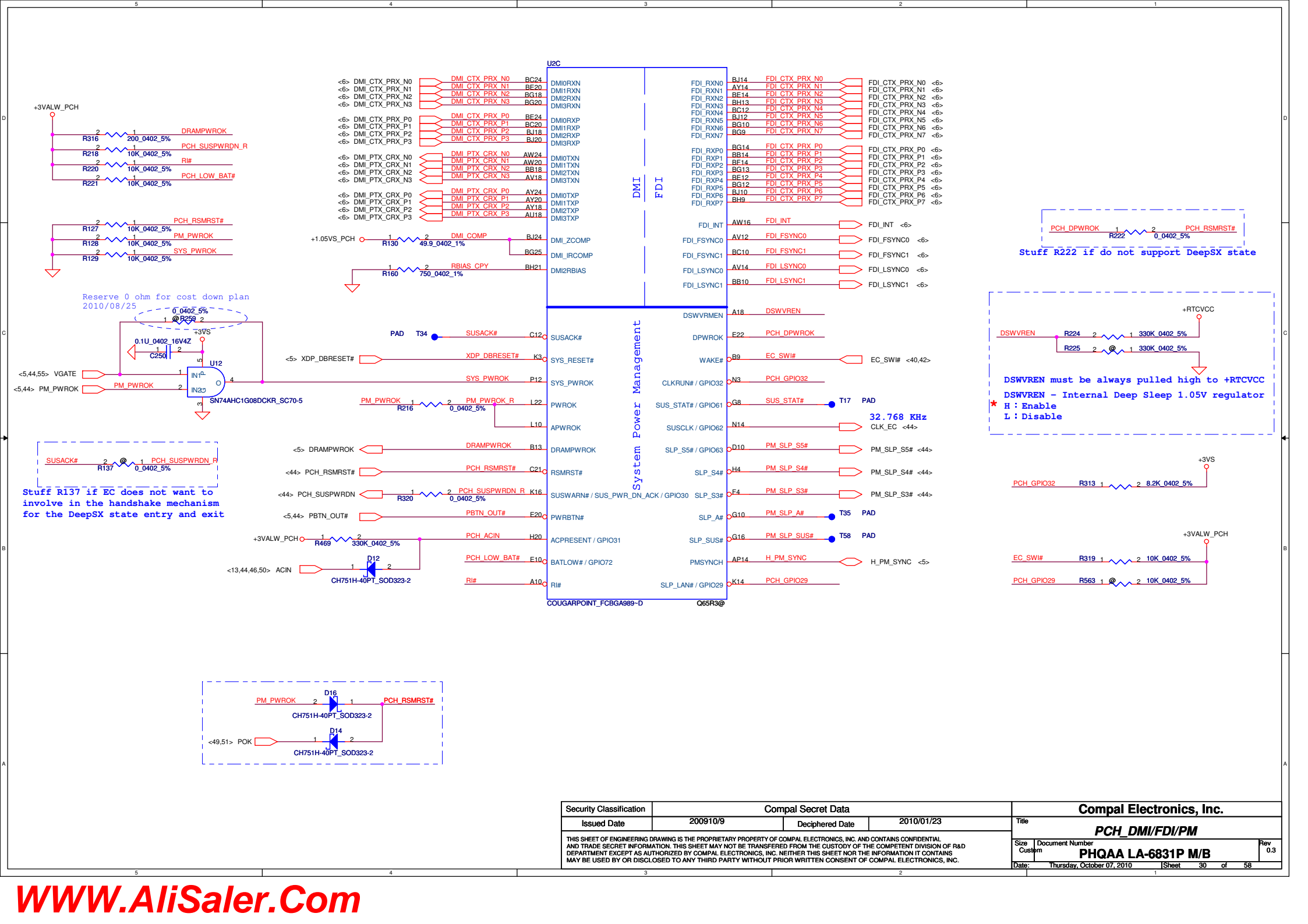
H=>On Die PLL is supplied by 1.5V

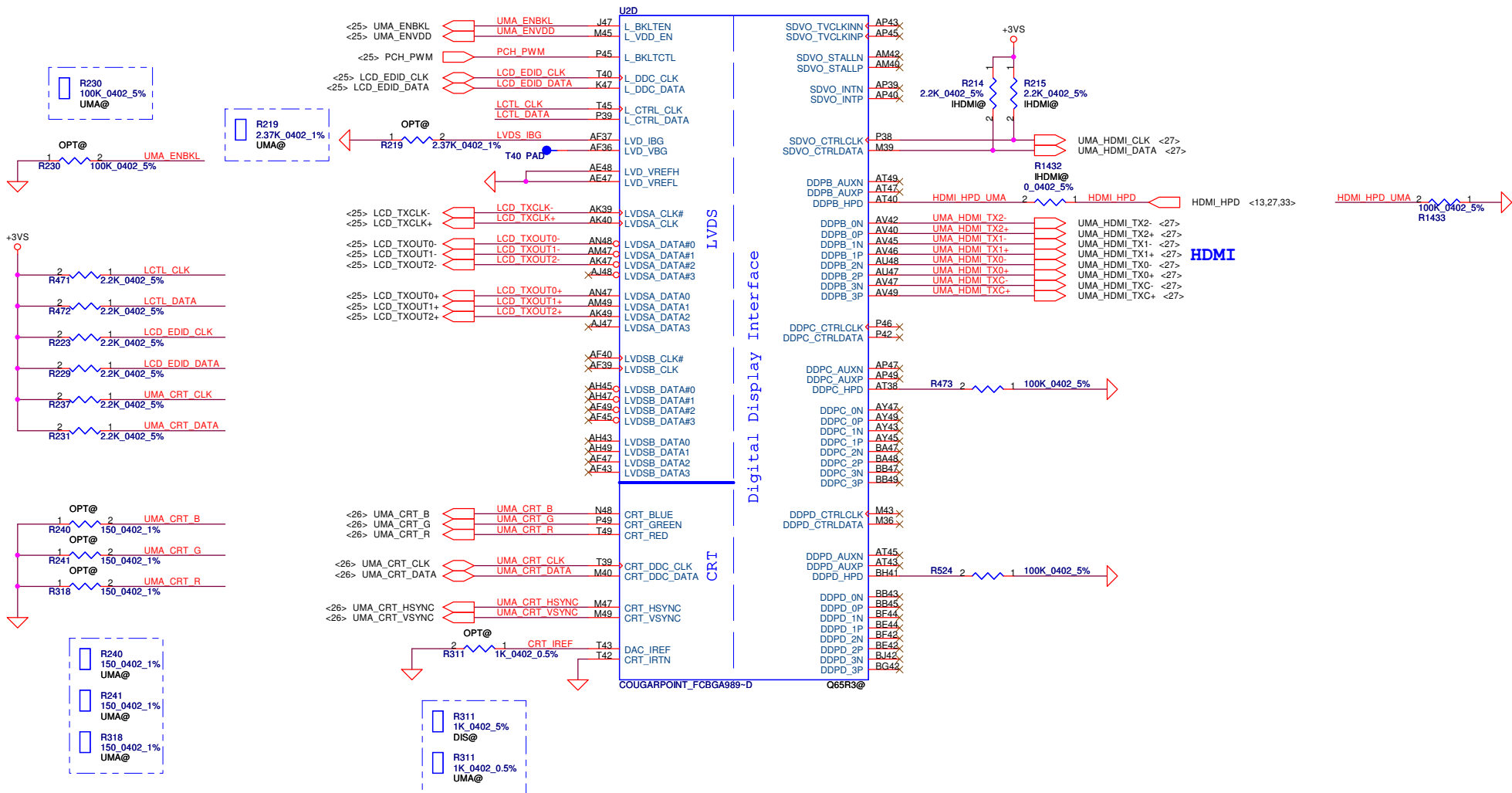
L=>On Die PLL is supplied by 1.8V

Need to pull high for Huron River platform

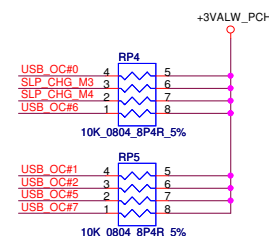
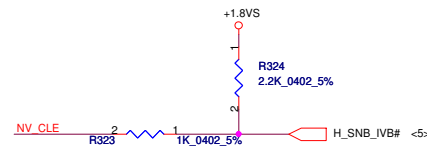
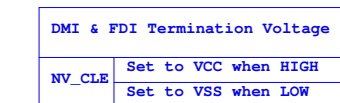
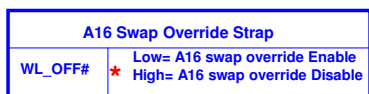
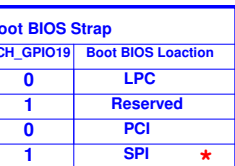
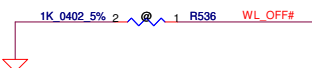
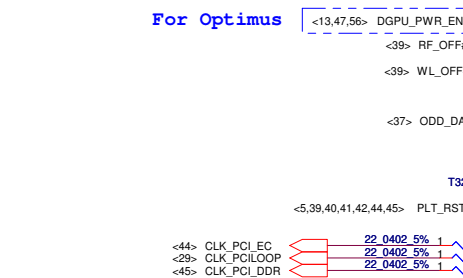






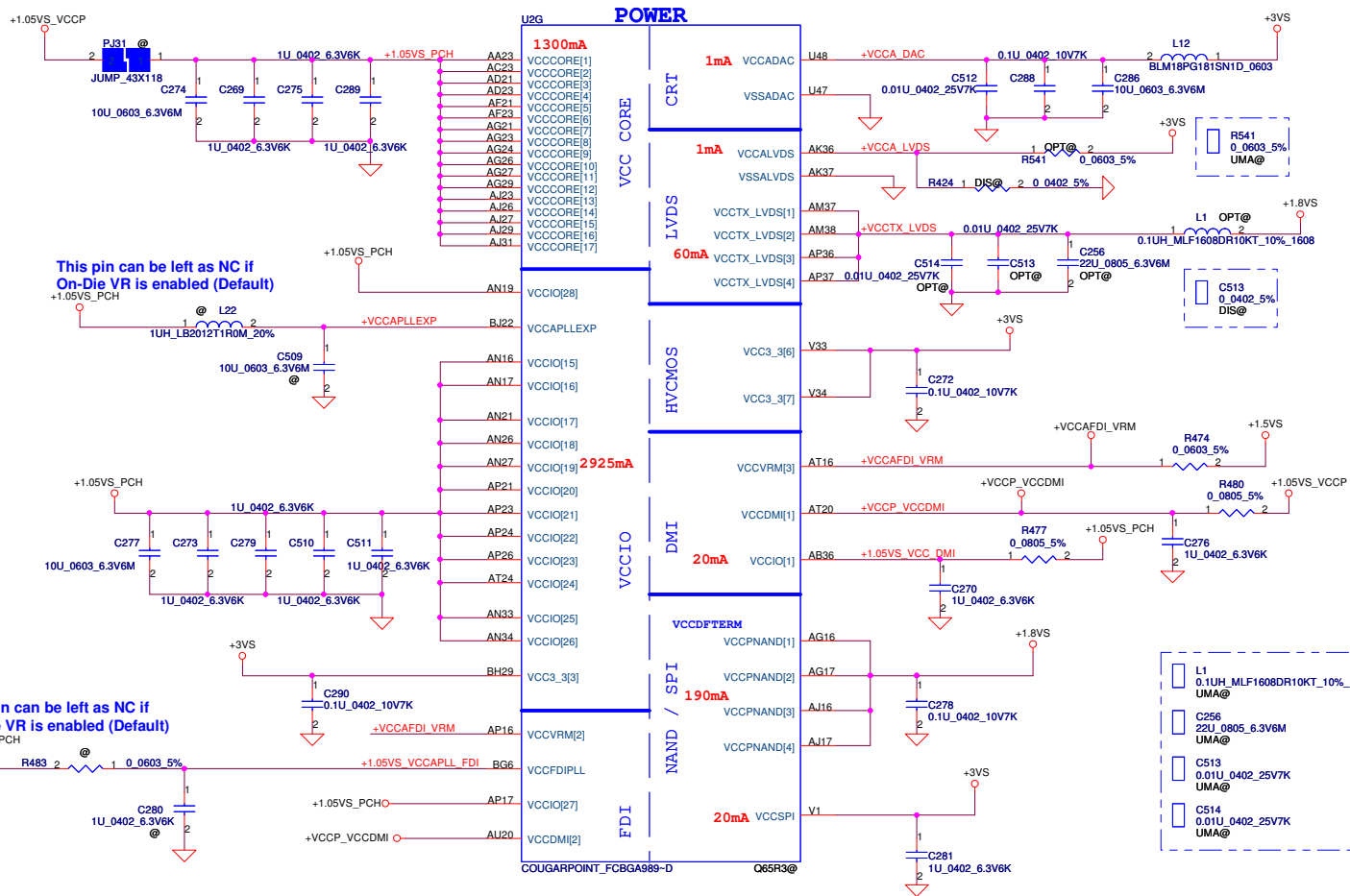


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	PHQAA LA-6831P M/B
				Date:	Thursday, October 07, 2010
				Sheet	31 of 58
				Rev	0.3

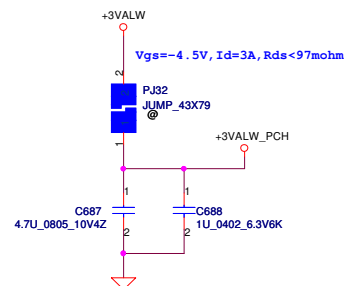


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	PCH_PCI/USB/NAND PHQAA LA-6831P M/B	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom	0.3
Date:	Thursday, October 07, 2010	Sheet	32	of	58

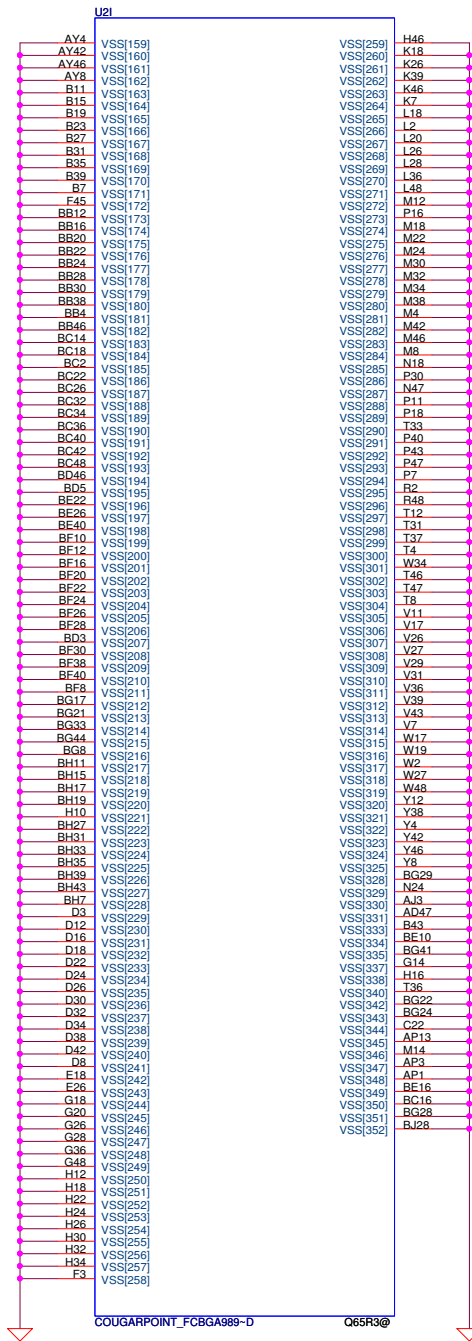
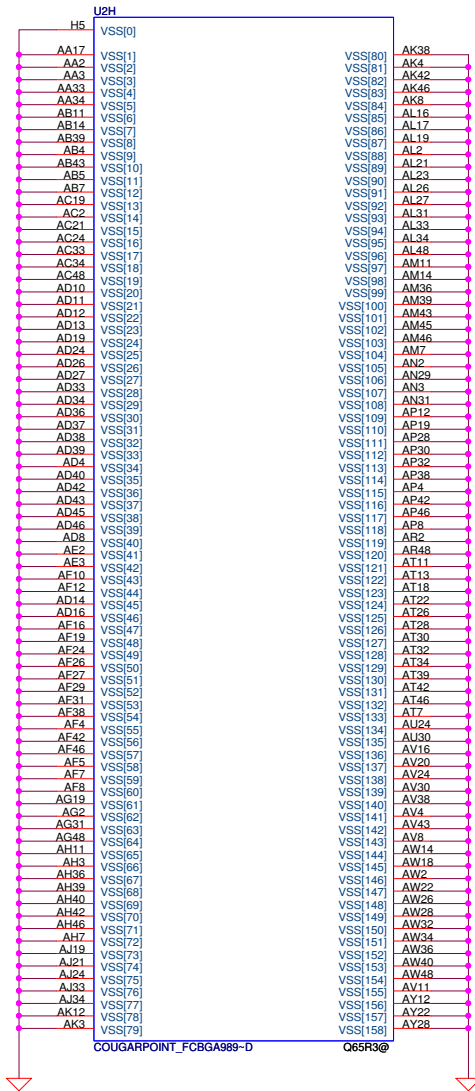




PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPILLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_POWER-1	
Size	Custom	Document Number	PHQAA LA-6831P M/B	Rev	0.3
Date	Thursday, October 07, 2010	Sheet	34	of	58



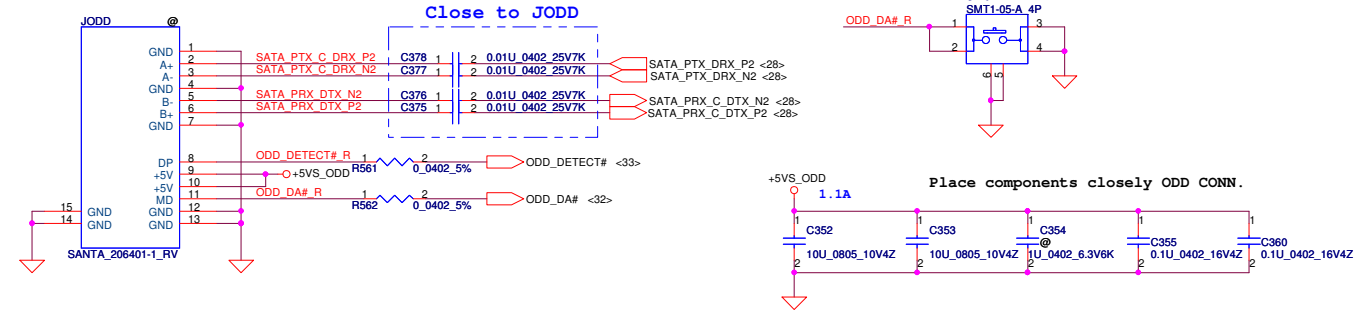
WWW.AliSaler.Com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_GND	
Size	Document Number	Rev			0.3
Custom	PHQAA LA-6831P M/B				
Date:	Thursday, October 07, 2010	Sheet	36	of	58

Place closely JHDD SATA CONN.

5VS 1.2A

C356 10U_0805_10V4Z C357 0.1U_0402_16V4Z C358 0.1U_0402_16V4Z C359 0.1U_0402_16V4Z



USB Board@ Right Side

W=60mils

For EMI

U14 RT9715BGS_008

C361 1000P_0402_50V7K

C362 4.7U_0805_10V4Z

+5VALW

+5V VCCA

+5V VIO

USB20_N0

USB20_P0

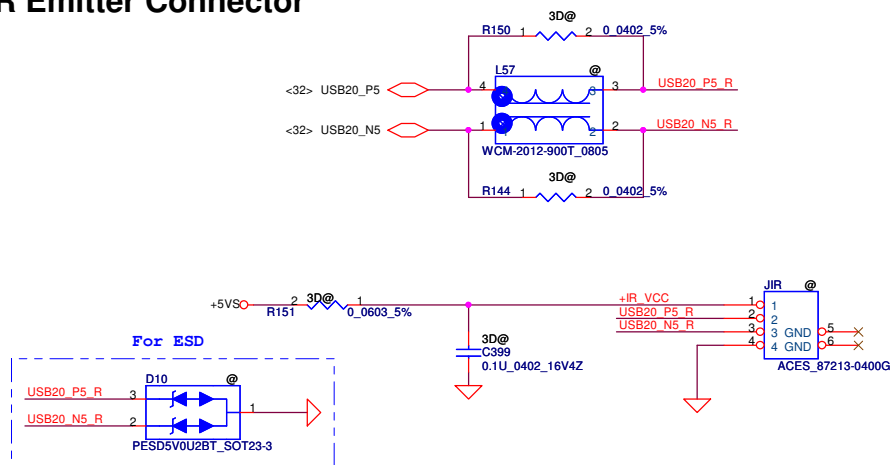
USB20_N1

USB20_P1

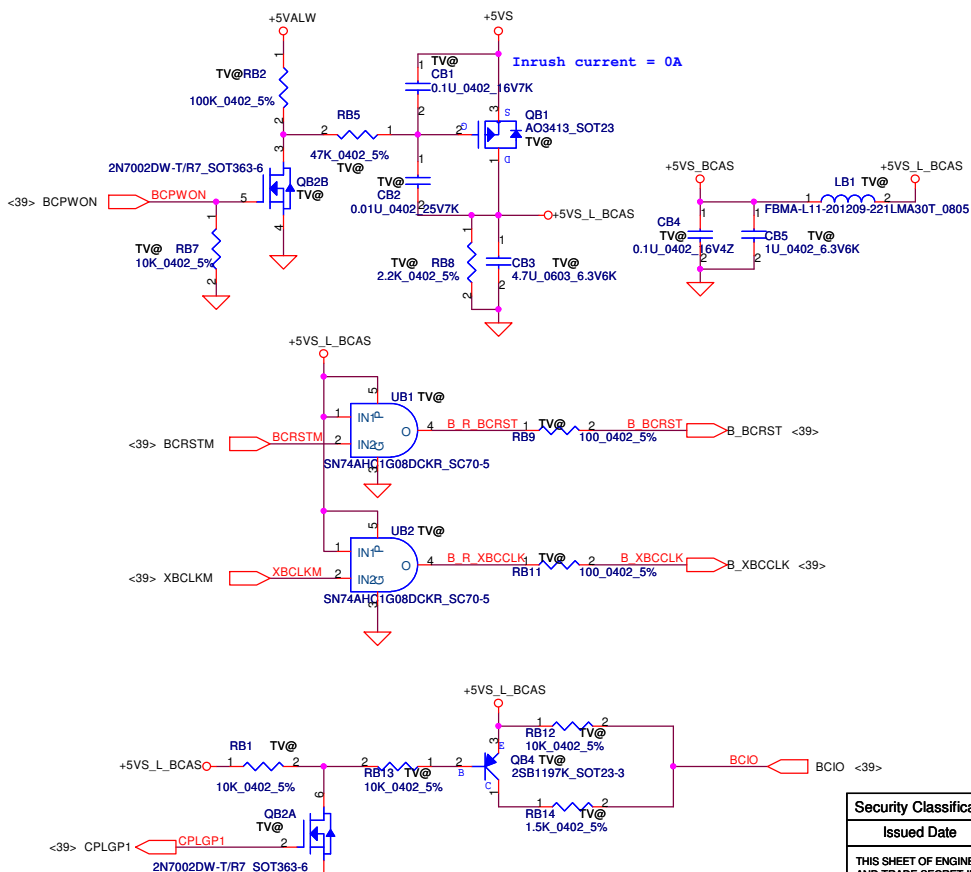
ACES_85201-2005N

WWW.AliSaler.Com

IR Emitter Connector

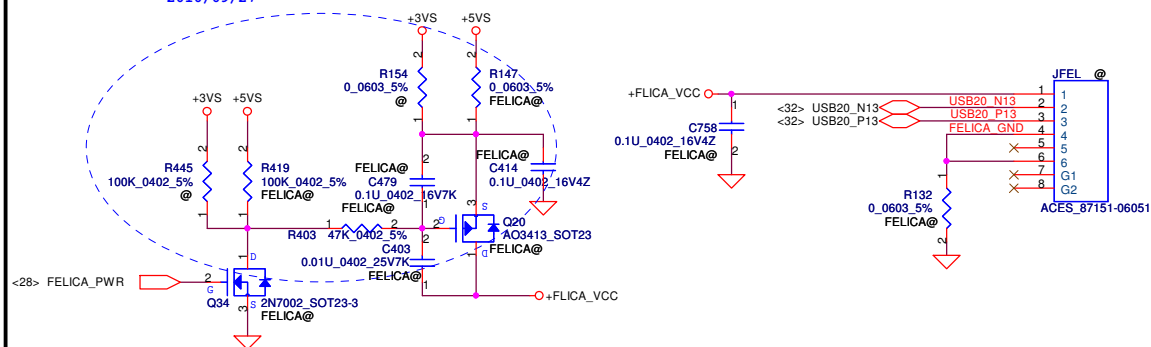


B-CAS Circuit

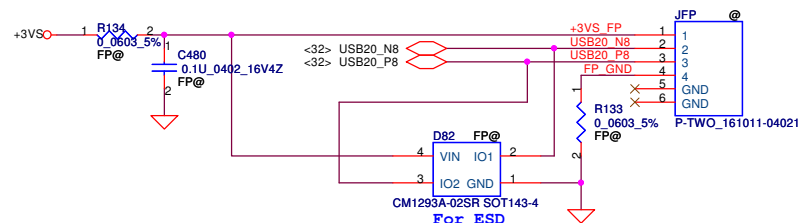


Felica

Reserve +3VS Felica by Customer demand.
2010/09/27



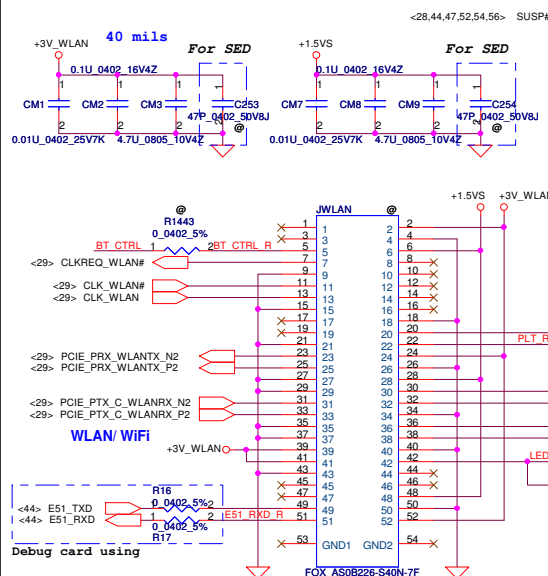
Finger printer



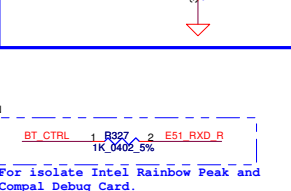
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		200910/9		Deciphered Date		2010/01/23		Title	
								IR/FP/B-CAS/Felica	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size		Document Number		Rev	
						PHQAA LA-6831P M/B		0.3	
Date:		Thursday, October 07, 2010		Sheet		38		of 58	

WLAN

Short PJ27 for Wimax
Short PJ26 for WLAN

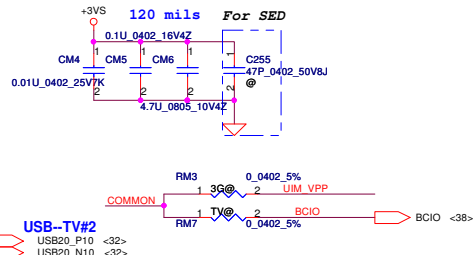
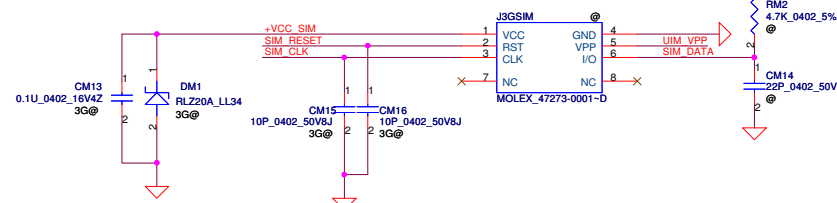


	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



The diagram illustrates the electrical connections between a PCIe controller (left) and a B-CAS component (right). The connections are as follows:

- PCIE-JET to B-CAS:**
 - BCCDET** (B-CAS pin 1) is connected to **PCIE<38> XBCLKM** (PCIE pin 3).
 - CLKREQ_JET#** (B-CAS pin 2) is connected to **PCIE<28> CLKREQ_JET#** (PCIE pin 7).
 - CLK_JET#** (B-CAS pin 29) is connected to **PCIE<29> CLK_JET#** (PCIE pin 11).
 - CLK_JET** (B-CAS pin 29) is connected to **PCIE<29> CLK_JET** (PCIE pin 13).
 - BCRST#** (B-CAS pin 38) is connected to **PCIE<38> BCRST#** (PCIE pin 17).
 - BCWPON** (B-CAS pin 38) is connected to **PCIE<38> BCWPON** (PCIE pin 19).
 - PCIE_PRX_JETTX_N3** (B-CAS pin 29) is connected to **PCIE<29> PCIE_PRX_JETTX_N3** (PCIE pin 21).
 - PCIE_PRX_JETTX_P3** (B-CAS pin 29) is connected to **PCIE<29> PCIE_PRX_JETTX_P3** (PCIE pin 23).
 - PCIE_PTX_C_JETRX_N3** (B-CAS pin 29) is connected to **PCIE<29> PCIE_PTX_C_JETRX_N3** (PCIE pin 31).
 - PCIE_PTX_C_JETRX_P3** (B-CAS pin 29) is connected to **PCIE<29> PCIE_PTX_C_JETRX_P3** (PCIE pin 33).
 - TMPTU2_SXP** (B-CAS pin 44) is connected to **PCIE<44> TMPTU2_SXP** (PCIE pin 47).
- B-CAS to PCIE-JET:**
 - ISDBT_DET** (B-CAS pin 18) is connected to **PCIE<33> ISDBT_DET** (PCIE pin 18).
 - RF_OFF#** (B-CAS pin 18) is connected to **PCIE<32> RF_OFF#** (PCIE pin 20).
 - PLT_RST#** (B-CAS pin 24) is connected to **PCIE<22> PLT_RST#** (PCIE pin 22).
 - USB20_P10_T1** (B-CAS pin 1) is connected to **PCIE<22> USB20_P10_T1** (PCIE pin 22).
 - USB20_N10_T1** (B-CAS pin 1) is connected to **PCIE<24> USB20_N10_T1** (PCIE pin 24).
 - USB20_N12** (B-CAS pin 32) is connected to **PCIE<32> USB20_N12** (PCIE pin 36).
 - USB20_P12** (B-CAS pin 32) is connected to **PCIE<32> USB20_P12** (PCIE pin 40).
 - CPLGP1** (B-CAS pin 46) is connected to **PCIE<38> CPLGP1** (PCIE pin 46).
 - TMPTU1_SXP** (B-CAS pin 44) is connected to **PCIE<44> TMPTU1_SXP** (PCIE pin 49).
- Other Connections:**
 - UIM_DATA** (B-CAS pin 2) is connected to **UIM_PWR** (PCIE pin 2).
 - UIM_CLK** (B-CAS pin 12) is connected to **UIM_PWR** (PCIE pin 12).
 - UIM_RESET** (B-CAS pin 14) is connected to **UIM_PWR** (PCIE pin 14).
 - COMMON** (B-CAS pin 16) is connected to **UIM_PWR** (PCIE pin 16).
 - LED_WIMAX#** (B-CAS pin 42) is connected to **UIM_PWR** (PCIE pin 42).
 - PM_SMBCLK** (B-CAS pin 30) is connected to **UIM_PWR** (PCIE pin 30).
 - PM_SMBDATA** (B-CAS pin 34) is connected to **UIM_PWR** (PCIE pin 34).
 - USB-3G/TV#1** (B-CAS pin 38) is connected to **UIM_PWR** (PCIE pin 38).
 - FOX_AS0B226-S40N-7F** (B-CAS pin 53) is connected to **UIM_PWR** (PCIE pin 53).



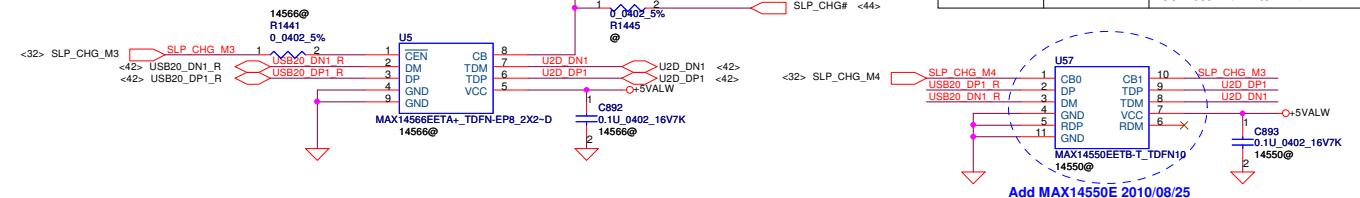
Pin connections for the SIM module:

- +5VS_BCAST (Pin 1) to +VCC_SIM (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).
- +UIM_PWR (Pin 1) to +VCC_SIM (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).
- UIM RESET (Pin 1) to SIM RESET (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).
- <38> B_BCRST (Pin 1) to UIM_CLK (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).
- UIM_CLK (Pin 1) to SIM_CLK (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).
- <38> B_XBCCLK (Pin 1) to UIM_DATA (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).
- UIM_DATA (Pin 1) to BCIO (Pin 2) via a 3GΩ resistor (0.0402_5% tolerance).

MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

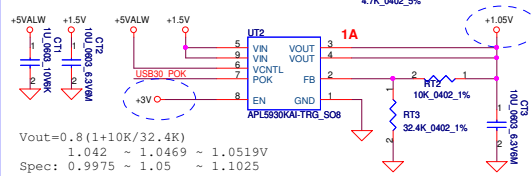
MAX14566E	
CB0: SLP_CHG_M4	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14550E		
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	MODE3
1	0	MODE4
1	1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

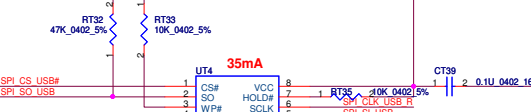
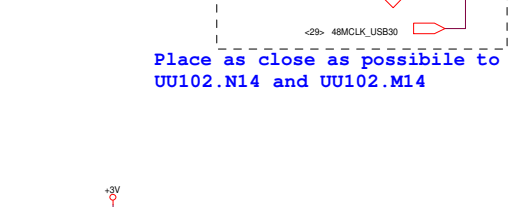
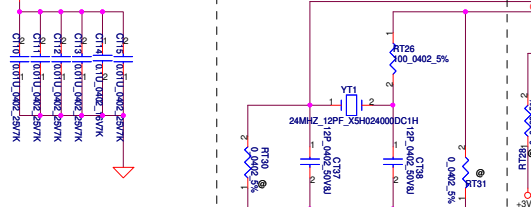
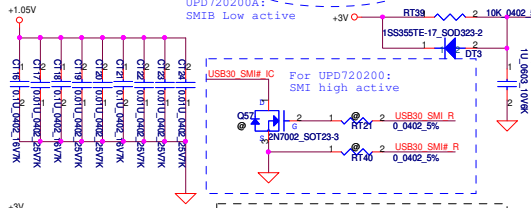
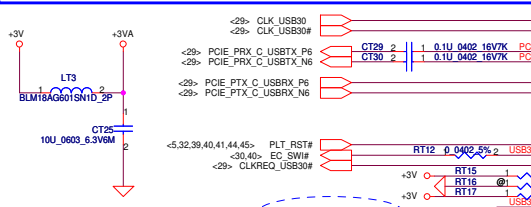
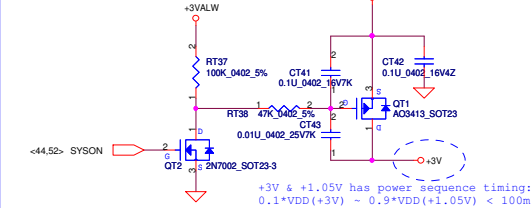


Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date	2009/01/9	Deciphered Date	2010/01/23	Title				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCIE-WLAN/JET/3G/TV/S&C				
				Size	Document Number			Rev
				PHQAA LA-6831P M/B				0.3
Date:	Thursday	October 07, 2010		Sheet	39	of	58	

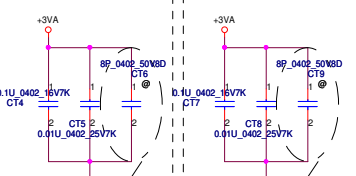
+1.5V to +1.05V Transfer



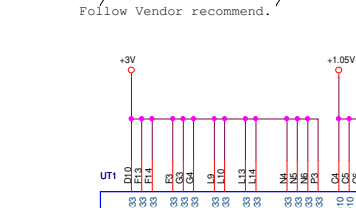
+3VALW to +3V Transfer



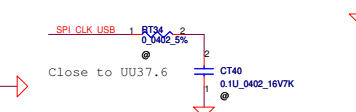
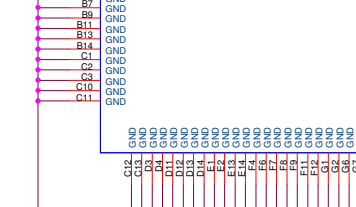
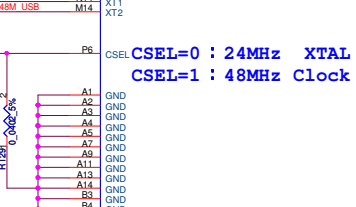
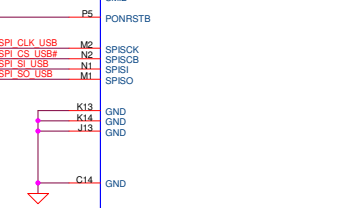
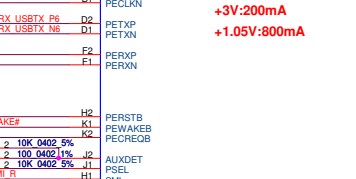
Close to U102.D7



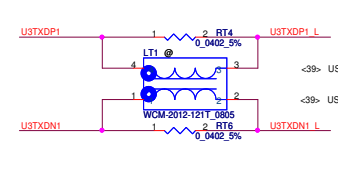
Close to U102.P13



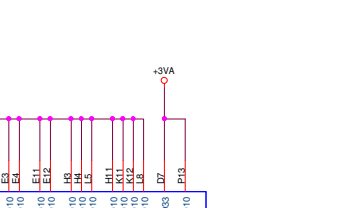
Follow Vendor recommend.



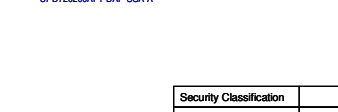
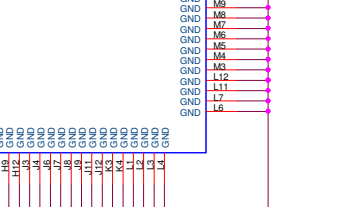
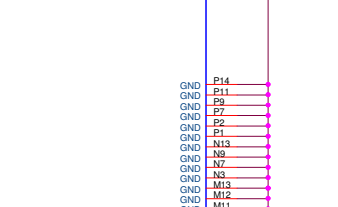
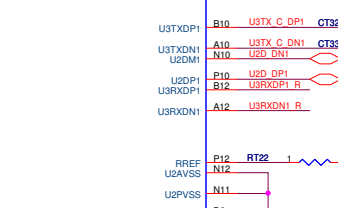
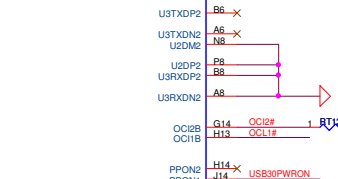
Close to U102.D7



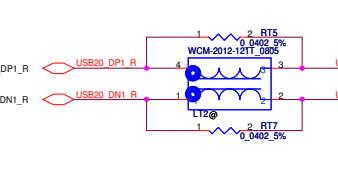
Close to U102.P13



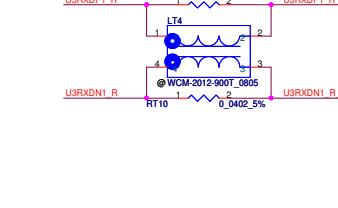
Follow Vendor recommend.



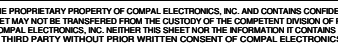
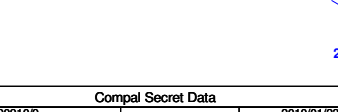
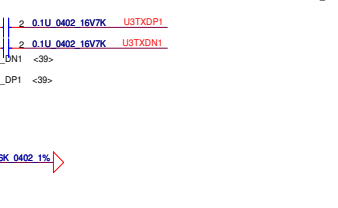
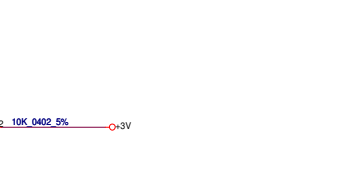
Close to U102.D7



Close to U102.P13



Follow Vendor recommend.



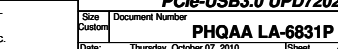
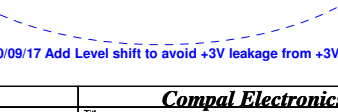
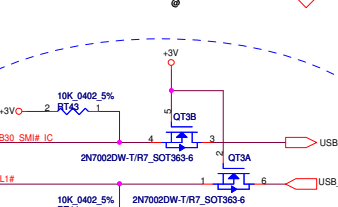
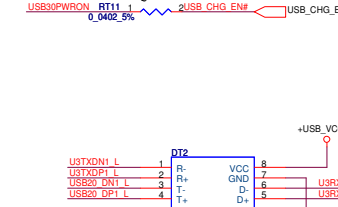
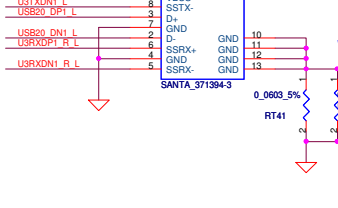
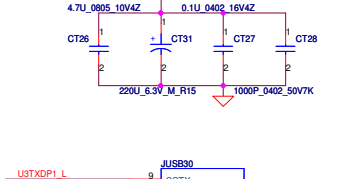
Close to U102.D7



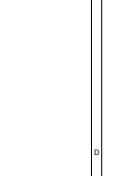
Close to U102.P13



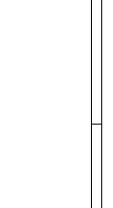
Follow Vendor recommend.



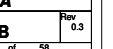
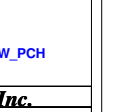
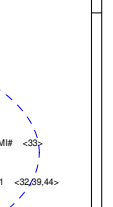
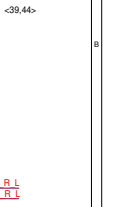
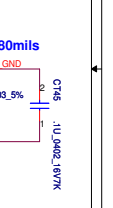
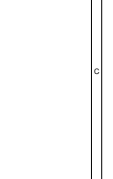
Close to U102.D7

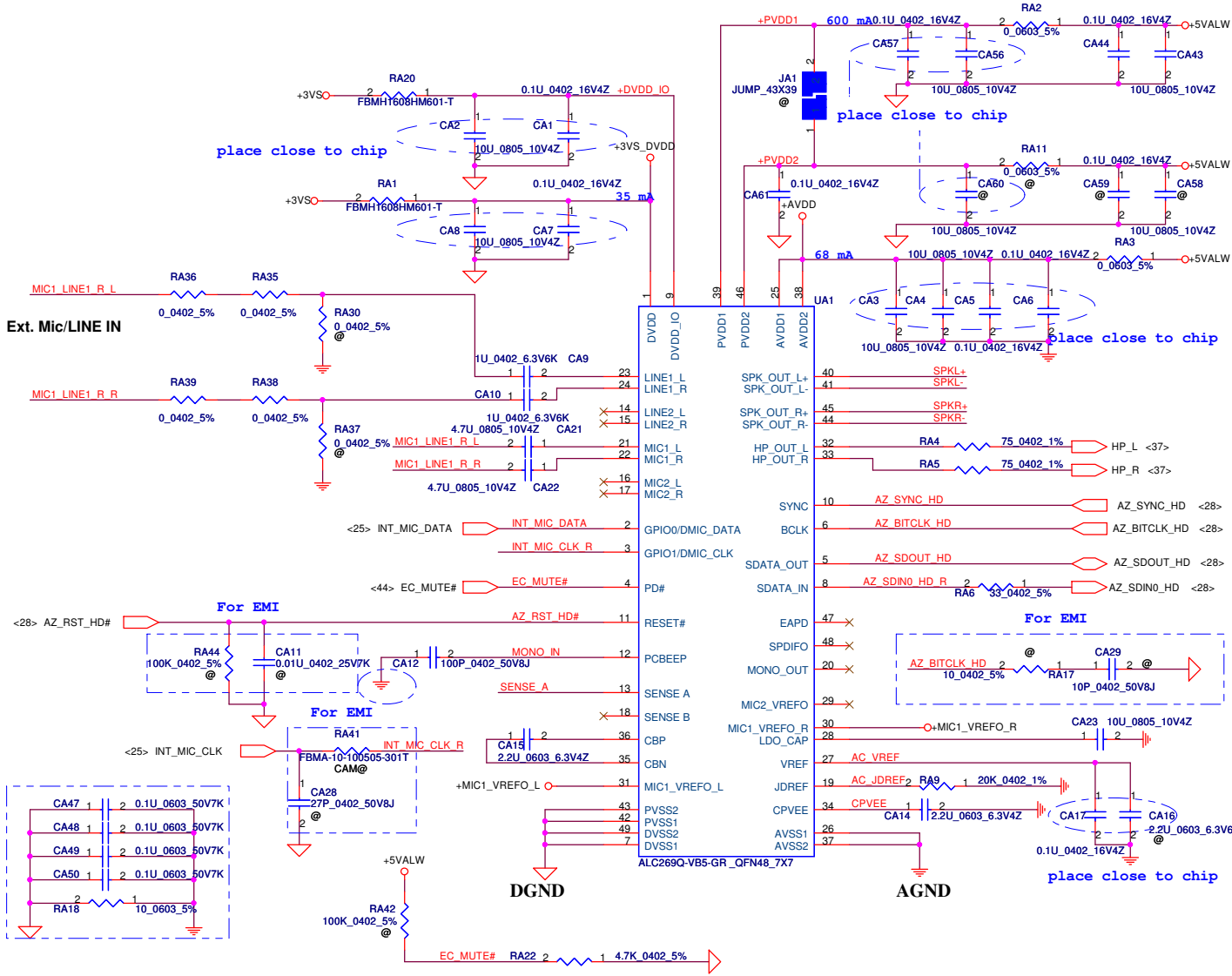


Close to U102.P13

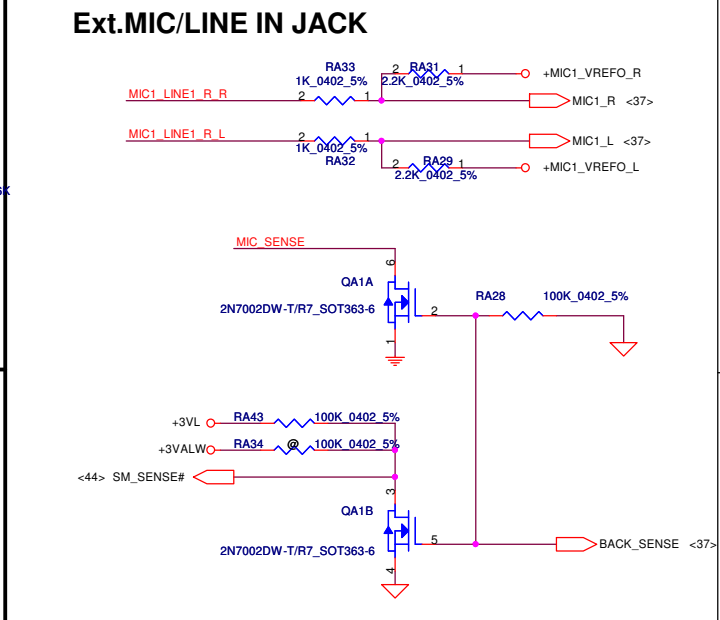
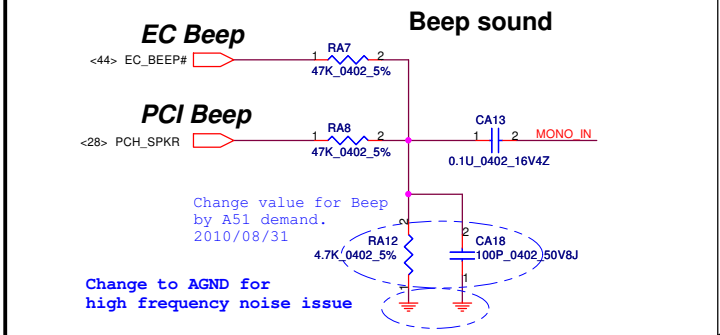
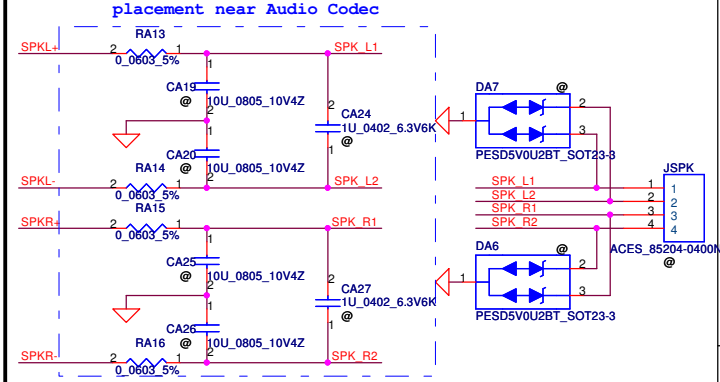


Follow Vendor recommend.

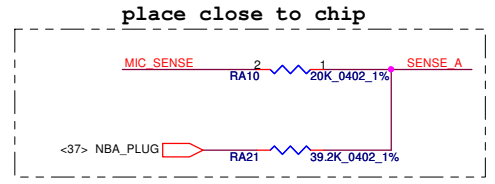




Speaker Connector

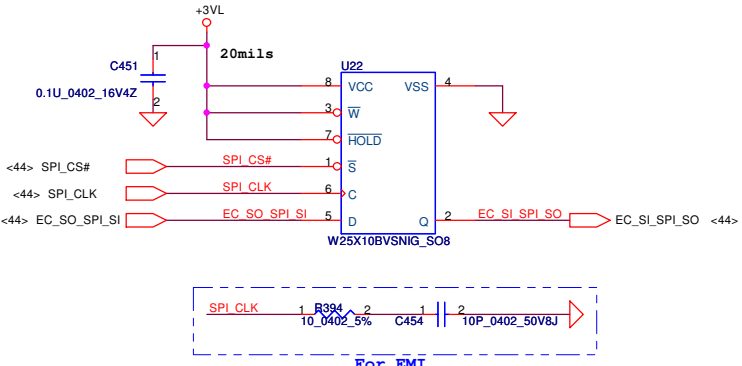


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

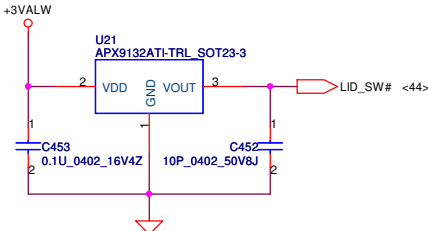


Security Classification		Compal Secret Data		Title	
Issued Date	2009/10/9	Deciphered Date	2010/01/23	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 0.3	
				Date: Thursday, October 07, 2010	
				Sheet 43 of 58	

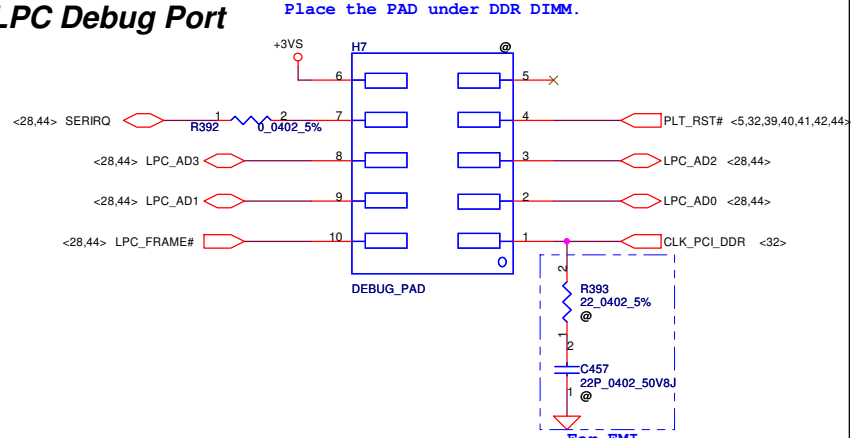
SPI Flash (256KB)



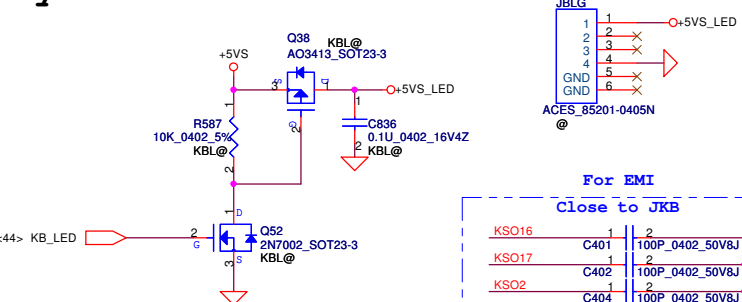
Lid SW



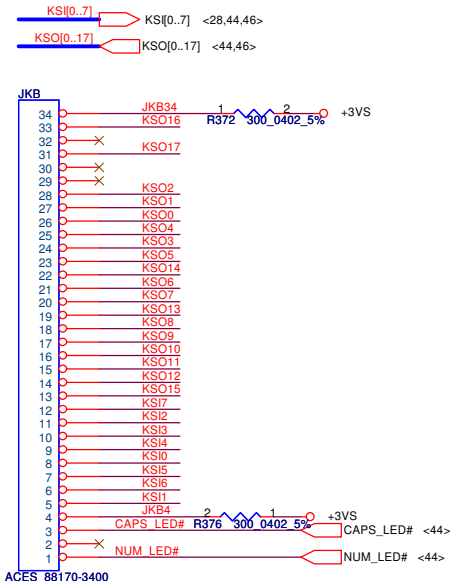
LPC Debug Port



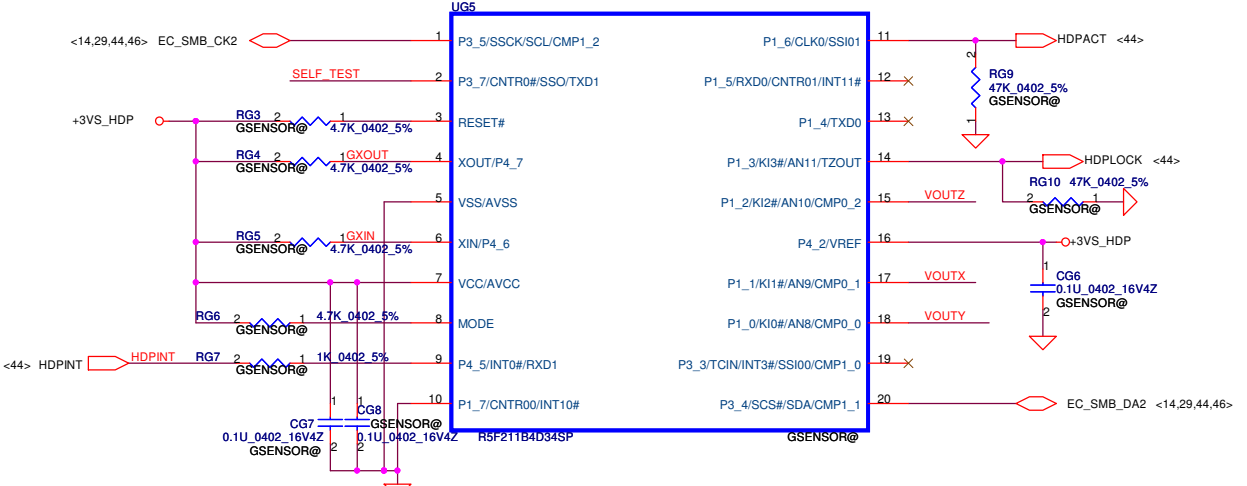
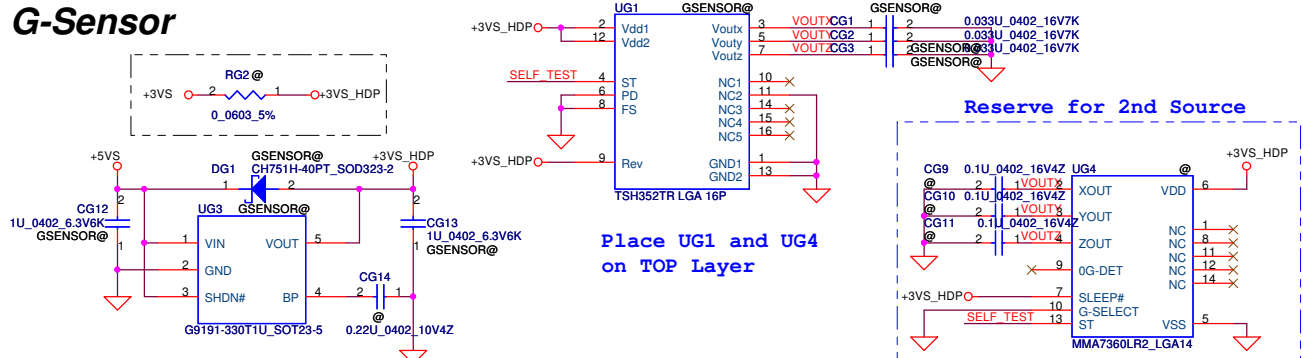
Keyboard LED



KEYBOARD CONN.

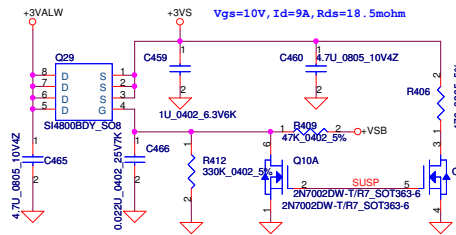


G-Sensor

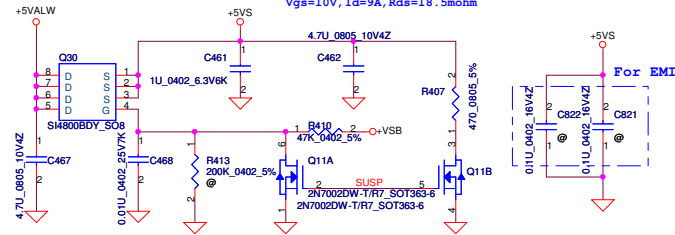


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SPI ROM/LID/Debug/KB/G-Sen	
				Size	Document Number
				PHQAA LA-6831P M/B	
Date		Thursday, October 02, 2010		Sheet	15 of 50

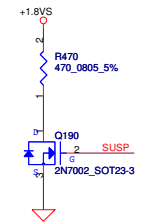
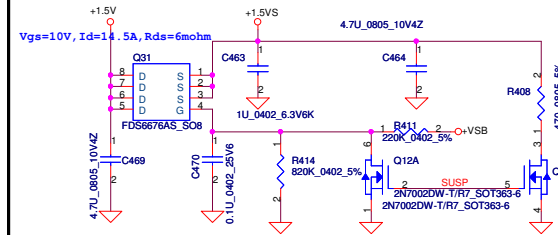
+3VALW TO +3VS



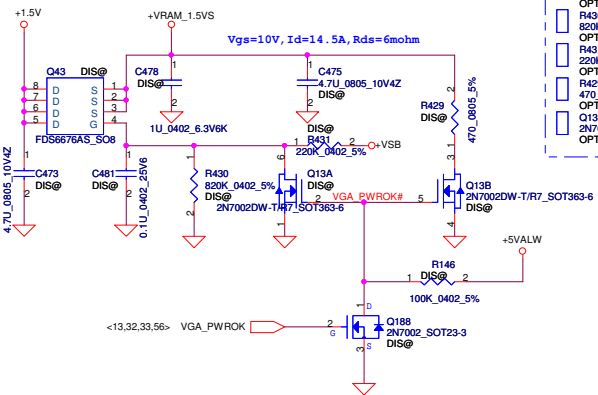
+5VALW TO +5VS



+1.5V to +1.5VS

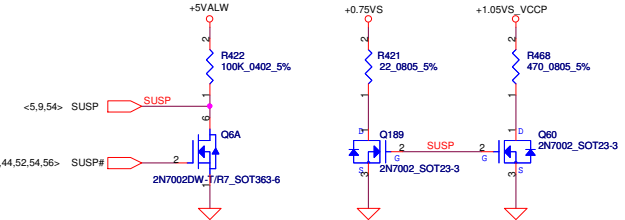
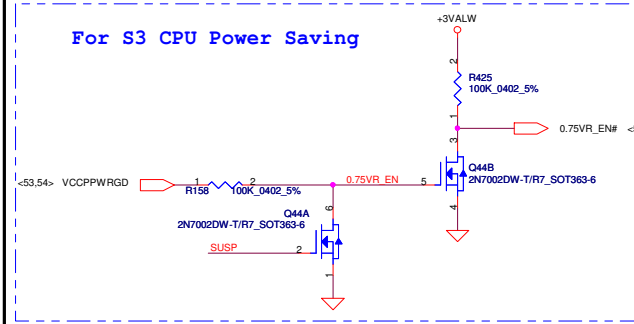


+1.5V to +VRAM_1.5VS

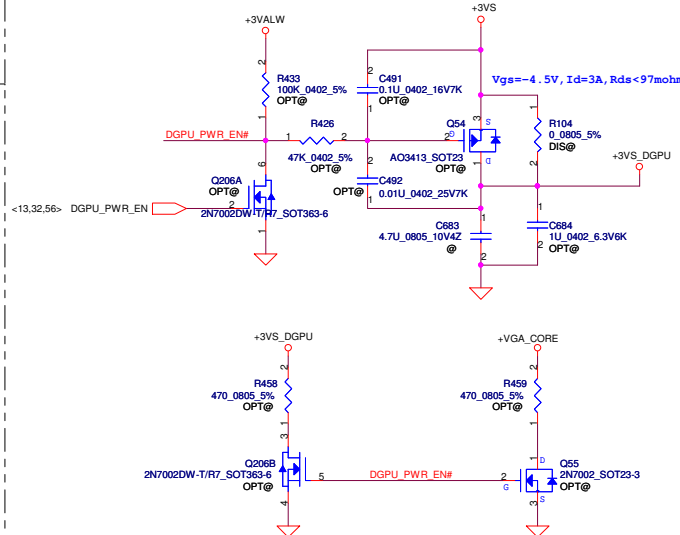


- | | | | |
|------|------------------------|------|----------------|
| Q43 | FDS6676AS_S08 | C473 | 470_0805_10V4Z |
| C481 | OPT@ | C479 | 1U_0402_6.3V6K |
| Q481 | OPT@ | C475 | 470_0805_10V4Z |
| R430 | 820K_0402_5% | C475 | 470_0805_10V4Z |
| R431 | 220K_0402_5% | C475 | 470_0805_10V4Z |
| R429 | 470_0805_5% | C475 | 470_0805_10V4Z |
| Q13 | 2N7002DW-T/R7_SOT363-6 | C475 | 470_0805_10V4Z |
| Q13 | 2N7002DW-T/R7_SOT363-6 | C475 | 470_0805_10V4Z |

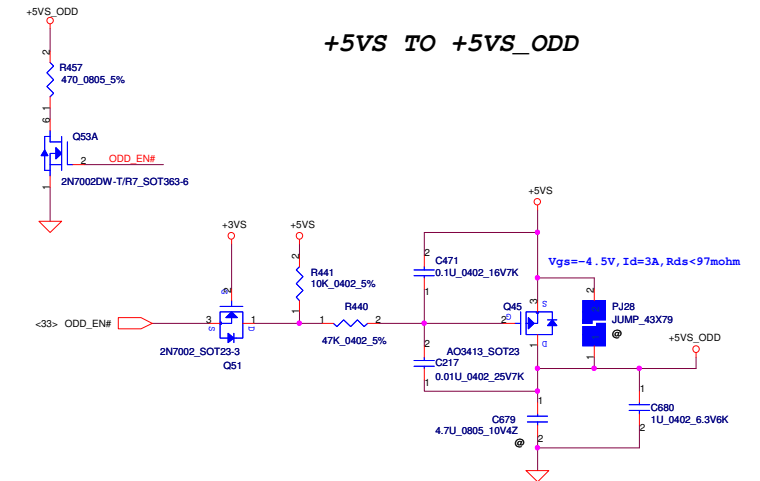
For S3 CPU Power Saving



+3VS to +3VS_DGPU

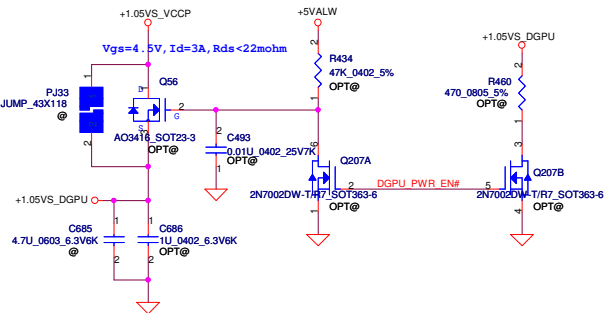


+5VS TO +5VS_ODD



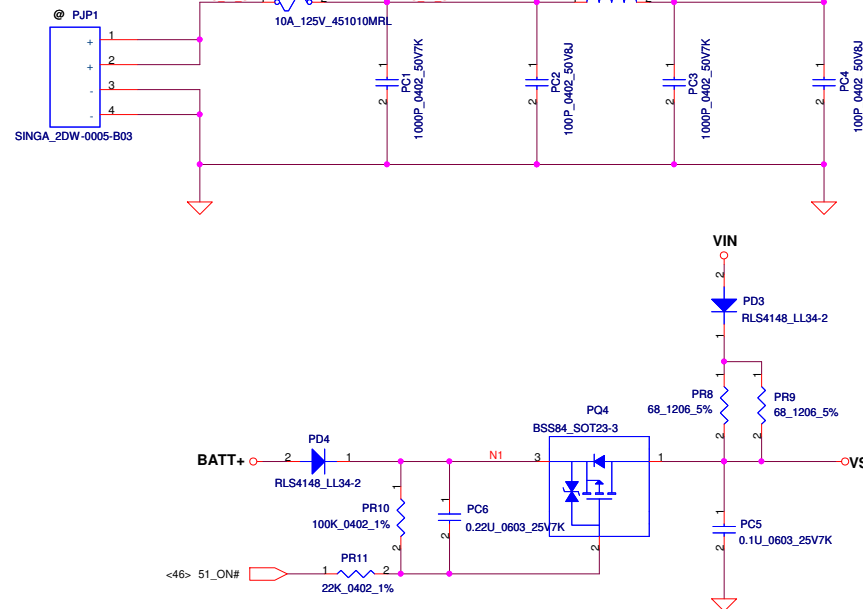
+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	DC-DC INTERFACE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 0.3
Date	Thursday, October 07, 2010	Sheet	47	of	58

DC301001M80



+3VALWP @ PJ332
JUMP_43X118
(5A, 200mils, Via NO.= 10)
OCP=7.7A

+0.75VSP @ PJ76
JUMP_43X79
(1A, 40mils, Via NO.= 2)

+5VALWP @ PJ352
JUMP_43X118
(5A, 200mils, Via NO.= 10)
OCP=7.9A

+VCCSAP @ PJ452
JUMP_43X118
(6A, 240mils, Via NO.= 12)
OCP=7A

+1.8VSP @ PJ182
JUMP_43X118
(1.65A, 70mils, Via NO.= 4)
OCP=4.2A

+3VLP @ PJ333
JUMP_43X39
(100mA, 40mils, Via NO.= 2)

+VSBP @ PJ2
JUMP_43X39
(120mA, 40mils, Via NO.= 1)

VL @ PJ353
JUMP_43X39
(100mA, 40mils, Via NO.= 2)

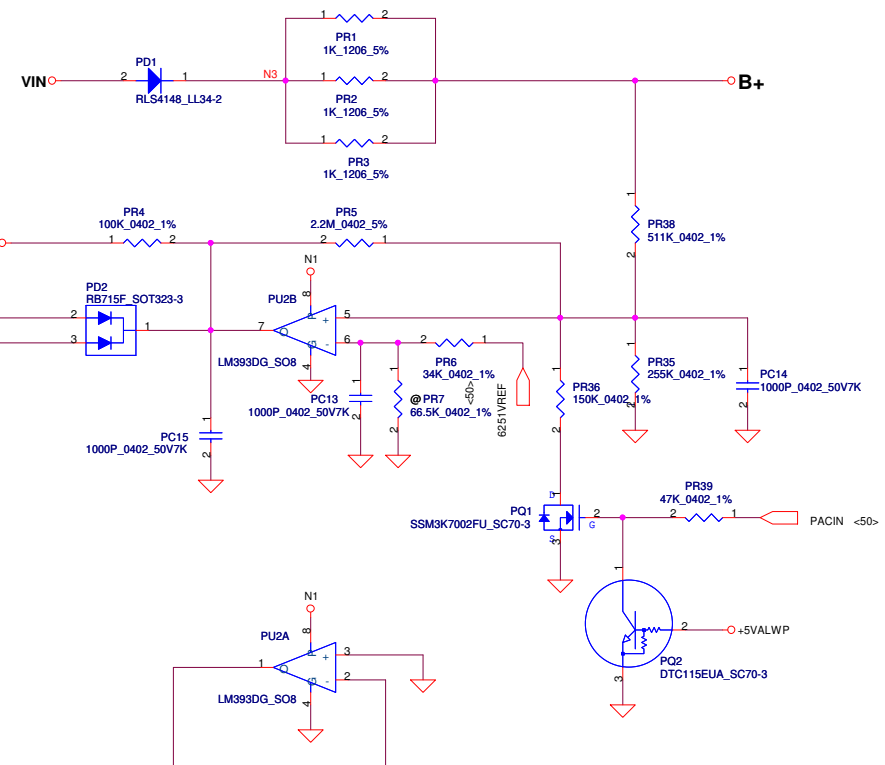
+VGA_COREP @ PJ602
JUMP_43X118
+VGA_CORE @ PJ603
JUMP_43X118
(30A, 1200mils, Via NO.=60)
OCP=39.62A

+1.5VP @ PJ152
JUMP_43X118
+1.5V @ PJ153
JUMP_43X118
(16A, 640mils, Via NO.= 32)
OCP=22.46

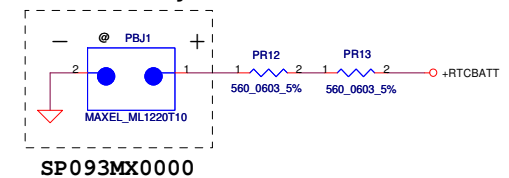
+1.05VS_VCCPP @ PJ402
JUMP_43X118
+1.05VS_VCCP @ PJ403
JUMP_43X118
(17A, 680mils, Via NO.=34)
OCP=19.23A

+GFX_COREP @ PJ502
JUMP_43X118
+GFX_CORE @ PJ503
JUMP_43X118
(33A, 1320mils, Via NO.=66)
OCP=40A

<51> EN0
<50> ACON



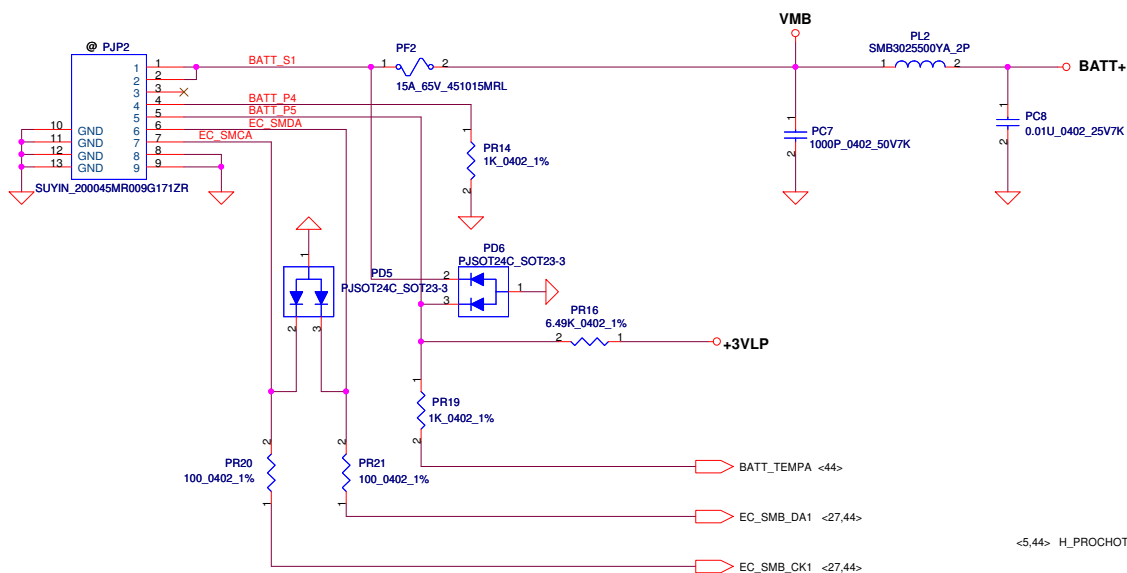
RTC Battery



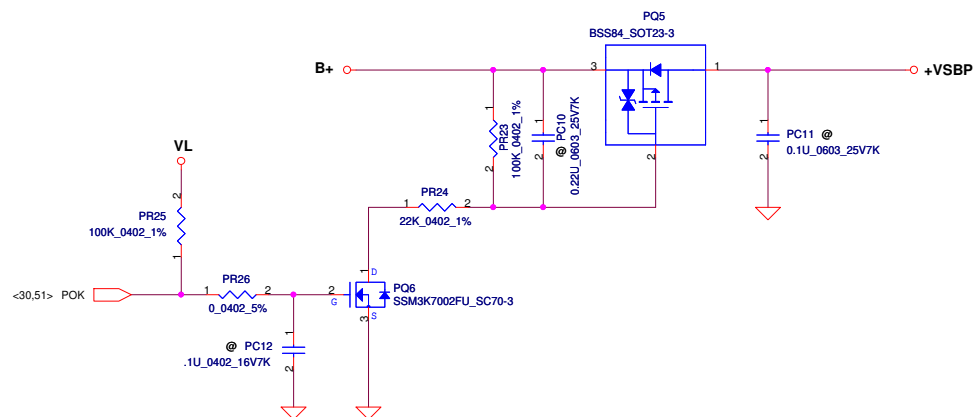
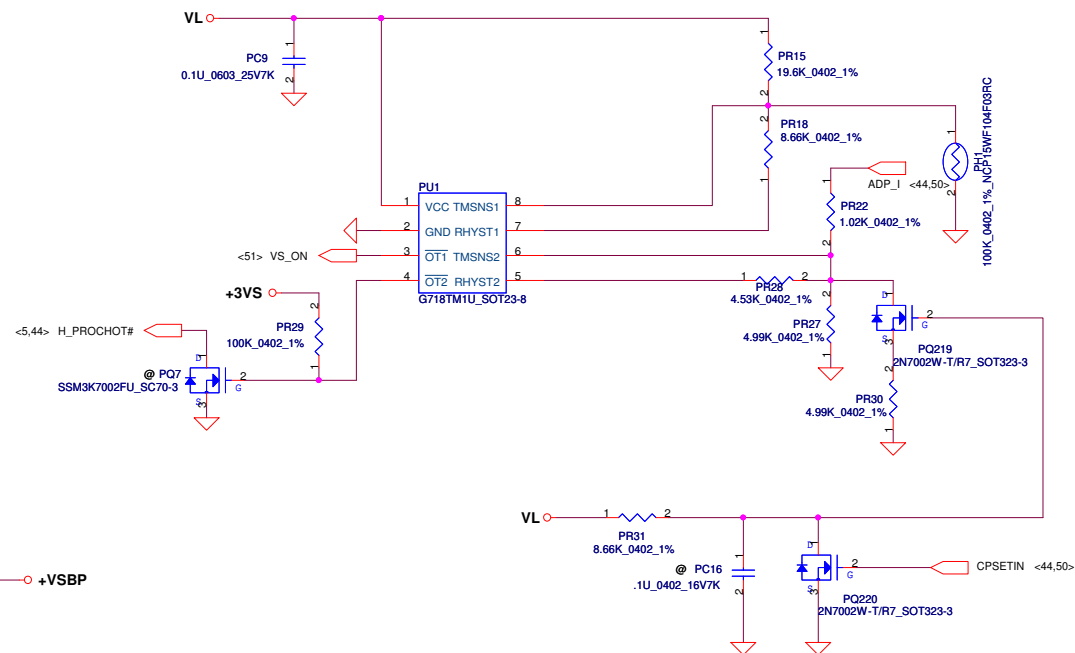
ACIN

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

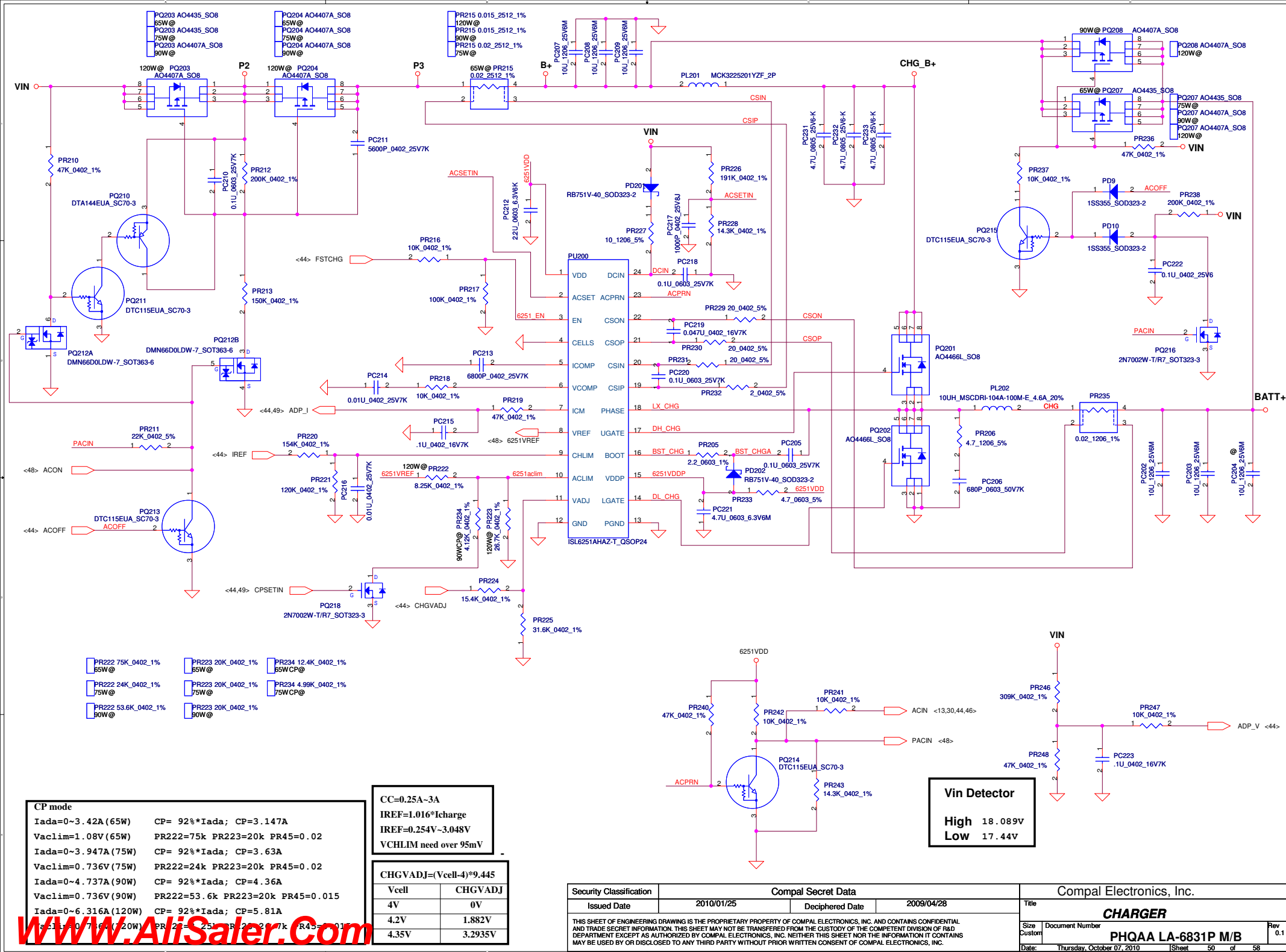
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title	DCIN/VIN DETECTOR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					PHQAA LA-6831P M/B	0.1
				Date:	Thursday, October 07, 2010	Sheet 48 of 58



PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				BATTERY CONN / OTP	
Size	Document Number	PHQAA LA-6831P M/B			Rev
Date:	Thursday, October 07, 2010	Sheet	49	of	58



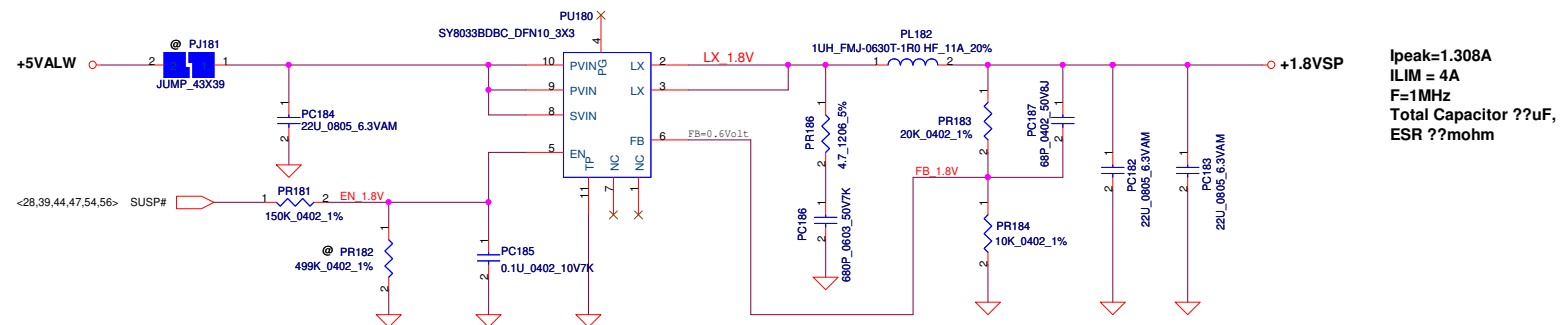
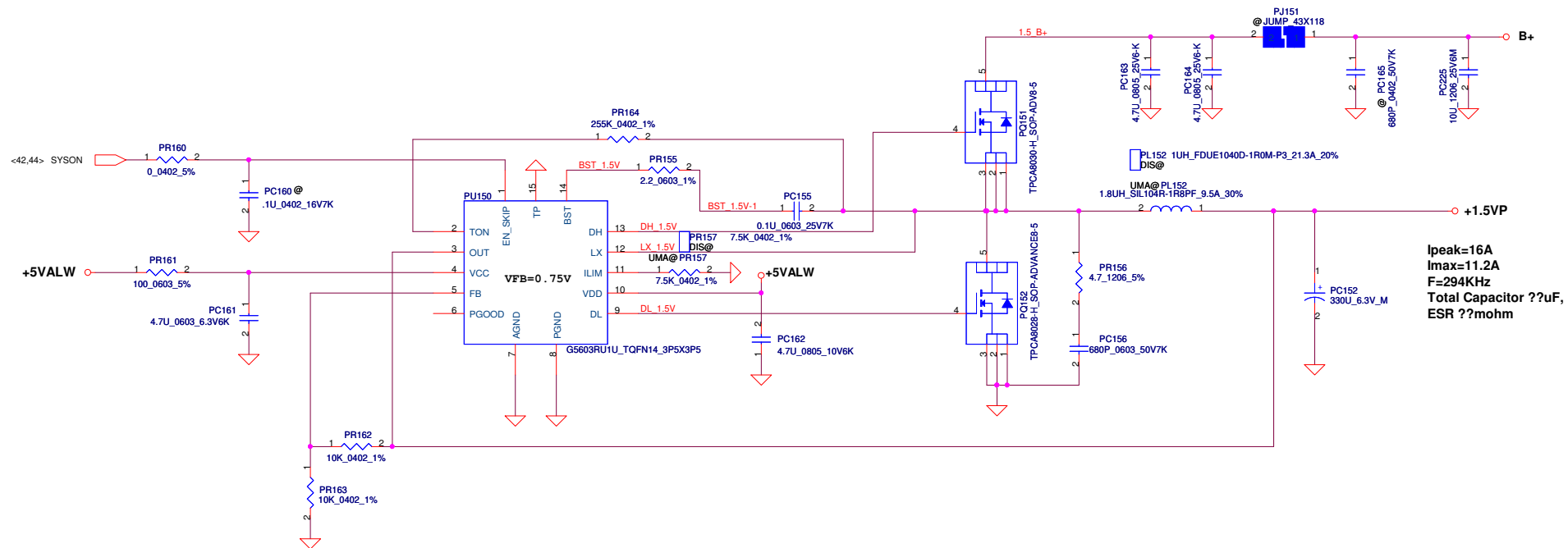
WWW.AliSaler.Com

CP mode
Iada=0~3.42A (65W) CP= 92%*Iada; CP=3.147A
Vaclim=1.08V (65W) PR222=75k PR223=20k PR45=0.02
Iada=0~3.947A (75W) CP= 92%*Iada; CP=3.63A
Vaclim=0.736V (75W) PR222=24k PR223=20k PR45=0.02
Iada=0~4.737A (90W) CP= 92%*Iada; CP=4.36A
Vaclim=0.736V (90W) PR222=53.6k PR223=20k PR45=0.015
Iada=0~6.316A (120W) CP= 92%*Iada; CP=5.81A
PR222=75k PR223=20k PR224=25k PR225=20k PR45=0.015

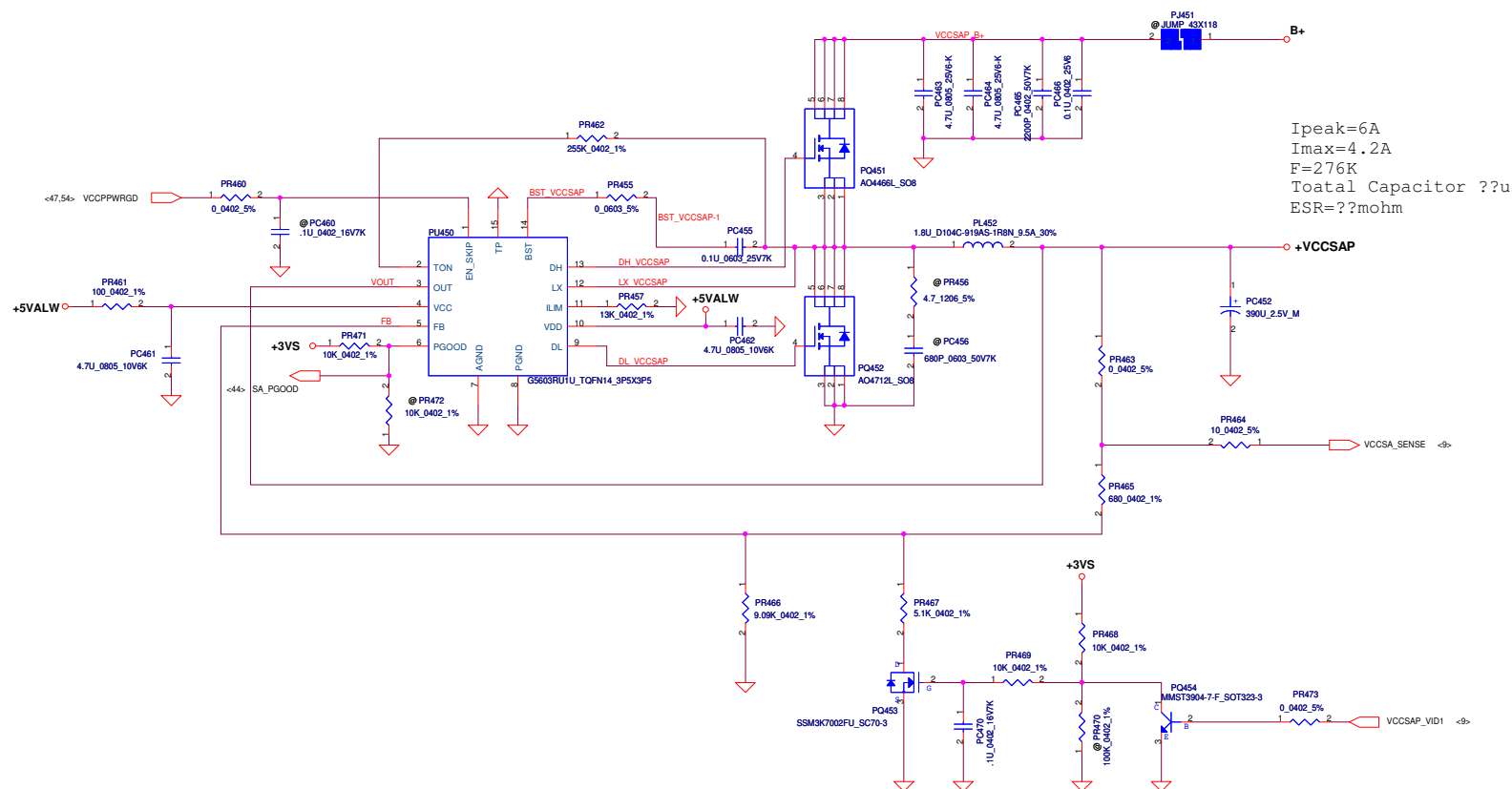
CC=0.25A-3A	
IREF=1.016*Icharge	
IREF=0.254V-3.048V	
VCHLIM need over 95mV	
CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Security Classification		Compal Secret Data	
Issued Date	2010/01/25	Deciphered Date	2009/04/28
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.			
Title			
CHARGER			
Size	Document Number	Rev	
Custom	PHQAA LA-6831P M/B	0.1	
Date:	Thursday, October 07, 2010	Sheet	50 of 58

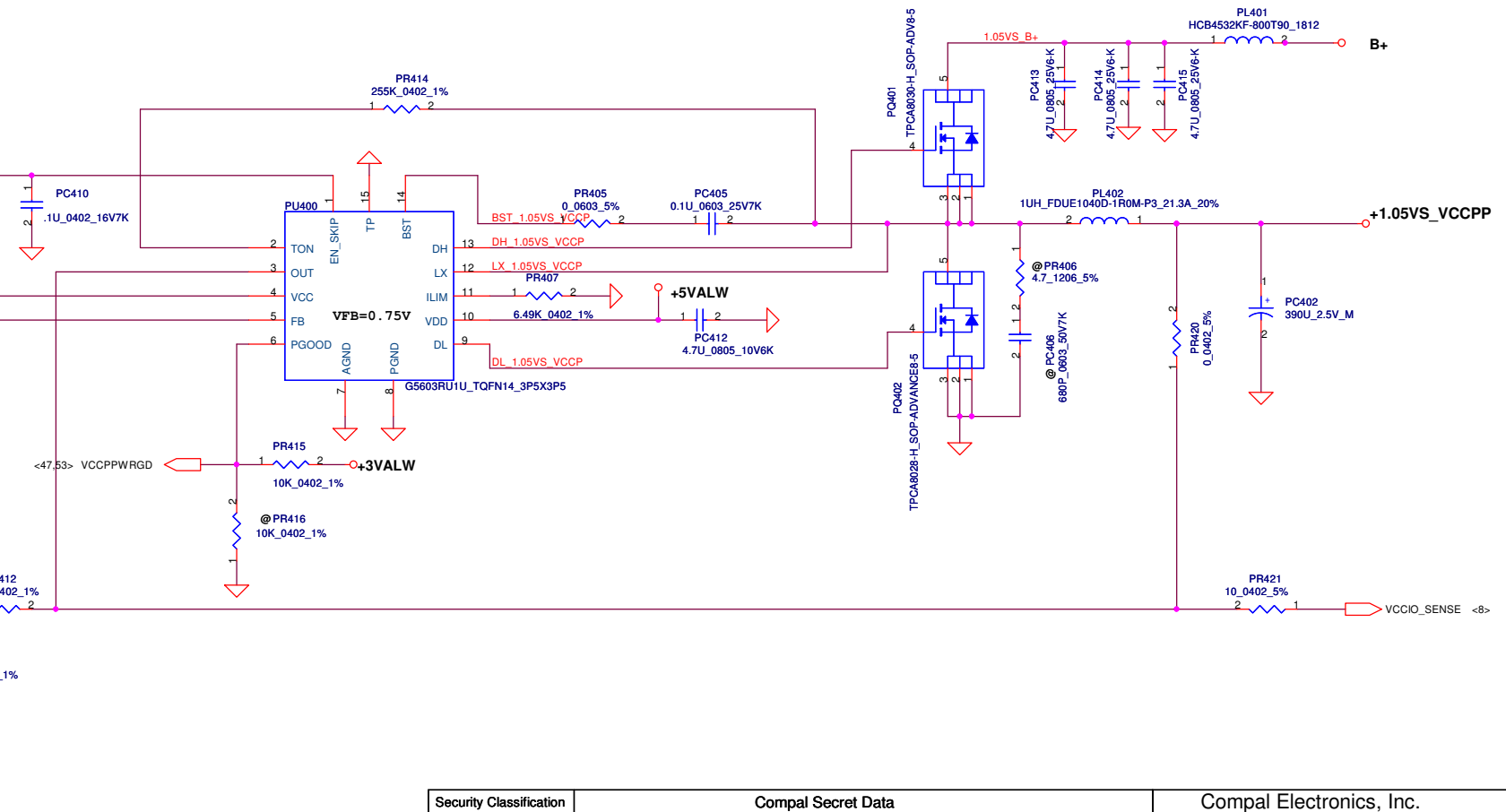
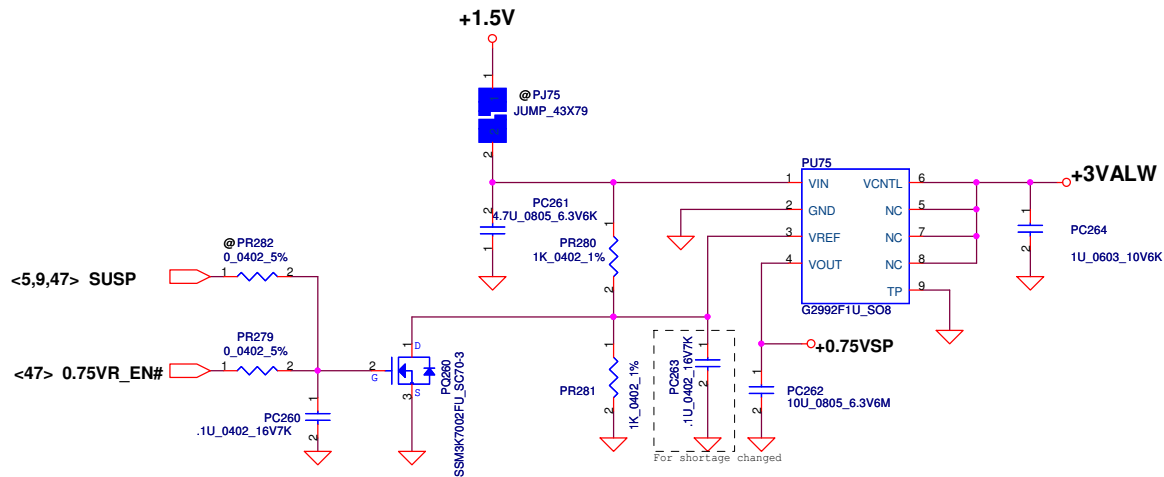


Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2010/01/25	Deciphered Date	2009/04/28	<div> <div>Title</div> <div>+1.5VP/+1.8VSP</div> </div>			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev	
				Custom	PHQAA LA-6831P M/B	0.1	
Date:				Thursday, October 07, 2010	Sheet	52	of 58

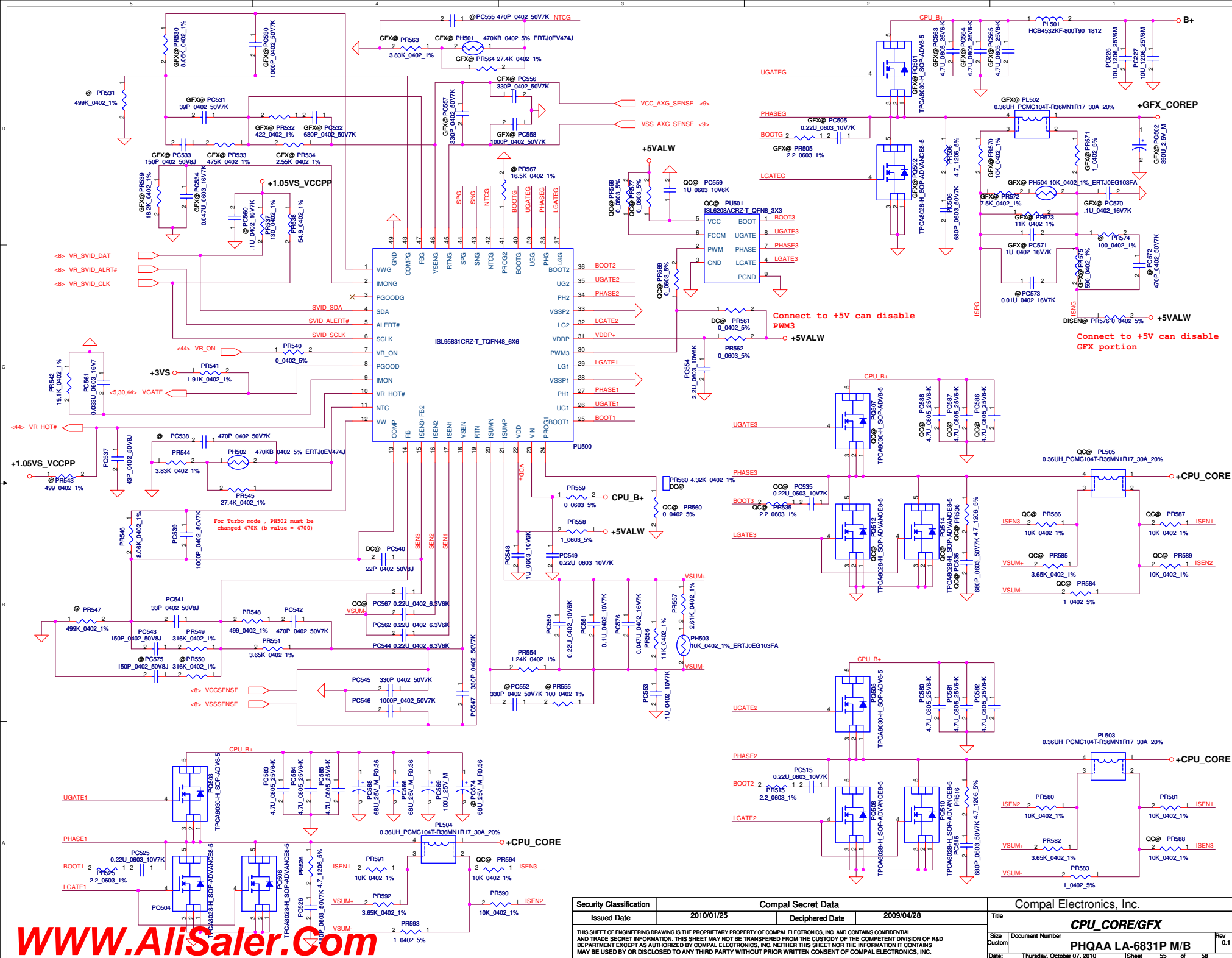


Ipeak=6A
 Imax=4.2A
 F=276K
 Toatal Capacitor ??u
 ESR=??mohm

VID1	+VCCSAP
1	0.8V
0	0.9V

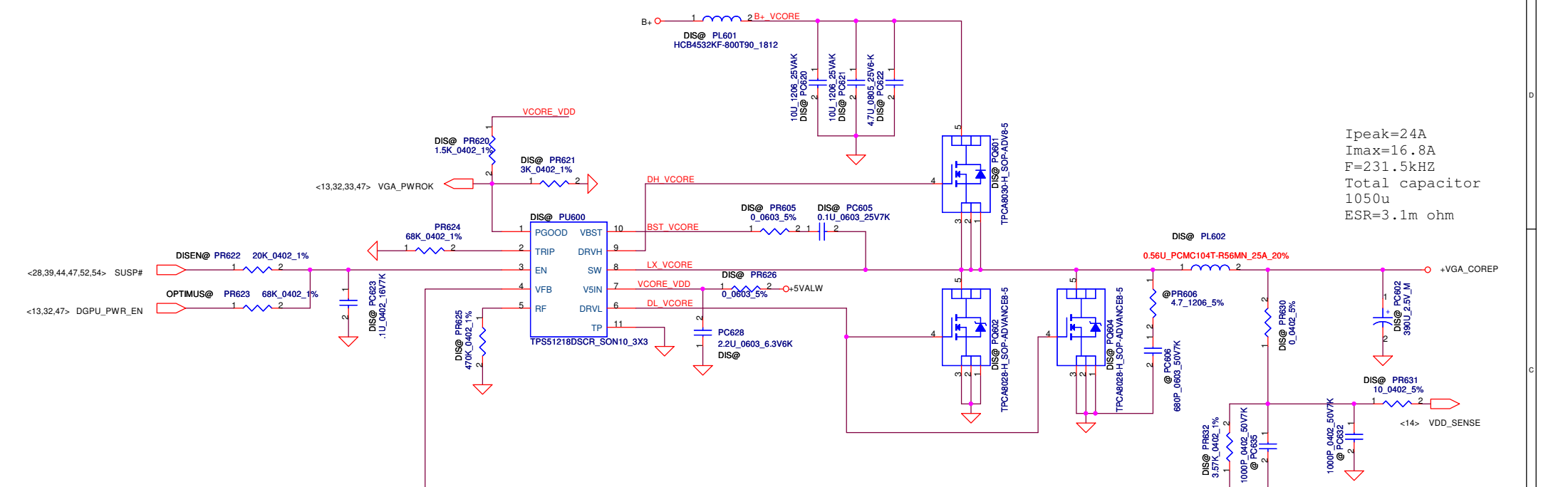


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				+1.05VS_VCCPP/+0.75VSP	
Size	Custom	Document Number	PHQAA LA-6831P M/B	Rev	0.1
Date:	Thursday, October 07, 2010	Sheet	54	of	58



WWW.AliSaler.Com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title	CPU_CORE/GFX
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				PHQAA	LA-6831P M/B
				Date	Thursday, October 07, 2010
				Sheet	55 of 58



Ipeak=24A
 Imax=16.8A
 F=231.5kHz
 Total capacitor
 1050u
 ESR=3.1m ohm

$FSW = 1 / (75E-12 * 57.6K) = 231.48KHz$

N12P-GV	N12P-GE	N12P-GS
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=32.14A
PR607=7.15K PQ604=unpop	PR607=7.15K PQ604=unpop	PR607=7.15K PQ604=unpop

$VFB(0.6) = Vout * Rbottom / (Rtop + Rbottom)$

Pstate	GPU_VID0	GPU_VID1	N12P-GV	N12P-LP	N12P-GS
P8/P12	0	0		0.825V	0.825V
P0 (hot)	1	0		0.9V	0.975V
	0	1			
P0 (cold)	1	1		0.925V	1V
				PR632=7.5K PR641=20K PR633=59K PR640=88.7K	PR632=7.5K PR641=20K PR633=59K PR640=88.7K

WWW.AliSaler.Com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
				+VGA_COREP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				PHQAA LA-6831P M/B	
				Date:	Thursday, October 07, 2010
				Sheet	56 of 58

HW PIR (Product Improve Record)

PHQAA LA-6831P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2010/09/03

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P08. Sandy Bridge_POWER-1	Remove C126, C131 and add C894 3Pin Bulk Cap Change C890, C891, C894 from SGA00005R00 (S POLY C 330U 2V M D2 LESR6M LX H1.9) to SGA00004X80 (S POLY C 470U 2V M D2 LESR4.5M LX H1.9) by Power demand.	By Power Transient test demand. By Power Transient test demand.
EVT		P13. VGA_PCIE/DAC/GPIO	Change RV8, RV9 to @ due to use internal thermal sensor.	Remove External Thermal and implement NV Internal Thermal sensor.
EVT		P14. VGA_LVDS/HDMI/THERM/eDP	Change External Thermal sensor UV2, CV53, CV54 to @. Change RV33, RV34 to always mount.	Remove External Thermal and implement NV Internal Thermal sensor. Remove External Thermal and implement NV Internal Thermal sensor.
EVT		P16. VGA_POWER	Change External Thermal sensor UV2, CV53, CV54 to @. Change RV33, RV34 to always mount.	Remove External Thermal and implement NV Internal Thermal sensor. Remove External Thermal and implement NV Internal Thermal sensor.
EVT		P28. PCH_HDA/JTAG/SATA/SPI/LPC	Change PWRME_CTRL# from PCH_GPIO33 to HDA_SDO. Remove R274. Change R442, R443 from 10k to 100k. Change U56 Pin3 from KSO6 to +5VALW. Add R227 100k ohm. Change U53 pin9 from KSI4 to KSI3. Change U13 from SA000021A00 to SA00003IN00.	Follow Intel Strap Pin Design Guide. Due to PCH GPIO33 no use. Modify SPI Debug Circuit. Due to EOL of SA000021A00
EVT		P29. PCH_PCI-E/SMBUS/CLK	Remover NEW Card Function: Remove PCIE interface.	A51 changed PRD Spec: remove New Card function
EVT		P30. PCH_DMI/FDI/PM	Reserve R259.	Cost down Plan
EVT		P32. PCH_PCI/USB/NAND	Remover NEW Card Function: Remove EXP_CPPE#	A51 changed PRD Spec: remove New Card function
EVT		P33. PCH_CPU/GPIO	Remove T73. Add USB Sleep & Charge MAXIC_Select pin in GPIO71.	Add USB Sleep & Charge IC detect function Add USB Sleep & Charge IC detect function
EVT		P37. SATA-HDD/ODD/USB	Change C426 to Aluminum Solid Cap 220uF	Cost Down Plan.
EVT		P39. PCIE-WLAN/JET/3G/TV/S&C	Remover NEW Card Function. Add USB Sleep & Charge IC: MAXI4550E. Add 14566@ & 14550@. Change U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4. Reserve R1443 for WLAN Mini PCIE Card Pin5.	A51 changed PRD Spec: remove New Card function Add USB Sleep & Charge IC MAXI4550E Set BOM Structure for MAXI4550E & MAXI4566B The conclusion of discussion with Sw Reserve for Broadcom combo card with BT
EVT		P40. PCIE-LAN-RTL8105E/8111E	Change 8105E-LDO@ to 8105ELDO@. Change 8105E-SWR@ to 8105ESWR@. Reserve DL1, D12 for ISN test by EMI demand. Add LL5 for ISN test by EMI demand. Add 16pin Xform for cost down, and P/N is SP050006E00	Avoid ISPD BOM Error Reserve for ISN Test by EMI demand Cost Down Plan
EVT		P41. PCIE-CardReader JMB389	Change JMB389@ to always mount.	Reduce BOM Config
EVT		P42. PCIE-USB3.0 UPD720200A	Change USB3.0 Connector Swap LT1 Add net name: SPI_CLK_USB_R.	ME demand. Layout demand. Layout demand.
EVT		P43. HDA-ALC269/HP/MIC	Change RA12 from 10k to 4.7kohm for Beep Change CA18 from 0.1uF tp 100pF for Beep	Let PC Beep to be clearer
EVT		P44. LPC-EC-KB930	Add CPSETIN function in EC_GPIO15.	Add it to detect QC/DC by Power demand.
EVT		P45. SPI ROM/LID/Debug/KB/G-Sen	Change EC ROM size from 256KB(SA00003GM10) to 128KB(SA00003FL10).	EC Cost down plan.
EVT		P46. PWR/Cap./TP/LED/LP/LS/Screw	Change SW1, SW4 to SN100002Y00.	

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	HW-PIR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				Date: Thursday, October 07, 2010	Sheet 57 of 57
				Rev 0.1	

1.	2010/08/12	P54-PWR-+1.05VS_VCCP/+0.75VSP	Change PU75 from UP7711 to G2992	Change source
2.	2010/08/12	P55-PWR-CPU_CORE/GFX	Change PU501 to SA000010200	Use Compal part number
3.	2010/08/12	P51-PWR_3VALWP/5VALWP	Change PU330 from UP6182CQAG to TPS51125A	Change source
4.	2010/08/12	P52-PWR-+1.5VP/+1.8VSP	Change PU150 from G5603 to RT8209B	Change source
5.	2010/08/12	P53-PWR-+VCCSAP	Change PU450 from G5603 to RT8209B	Change source
6.	2010/08/12	P54-PWR-+1.05VS_VCCP/+0.75VSP	Change PU400 from G5603 to RT8209B	Change source
7.	2010/08/12	P50-PWR-CHARGER	Change PQ204 from A04435 to A04407	Increase current margin for back to back MOS
8.	2010/08/12	P48-PWR_DCIN/VIN DECTOR	Change PQ1,PQ4 to SB900840003	For shortage issue
9.	2010/08/12	P49-PWR_BATTERY CONN / OTP	Change PQ5 to SB900840003	For shortage issue
10.	2010/08/12	P55-PWR-CPU_CORE/GFX	Add PR544 3.83k,PR545 27.4k,PH502 470k	For CPU NTC function
11.	2010/08/12	P55-PWR-CPU_CORE/GFX	Add PR560 0 Ohm	Set CPU VBOOT to 0V
12.	2010/08/12	P52-PWR-+1.5VP/+1.8VSP	Change PR157 10k to 7.5k	For DIS OCP(22.46A)
			Change PR157 10k to 4.7k	For UMA OCP(13.96A)
13.	2010/08/12	P53-PWR-+VCCSAP	Change PR457 10k to 13k	Set OCP(7A)
14.	2010/08/12	P54-PWR-+1.05VS_VCCP/+0.75VSP	Change PR407 13.7k to 6.49k	Set OCP(19.23A)
15.	2010/08/12	P51-PWR_3VALWP/5VALWP	Change PC332, PC352 to 330U	Change source
16.	2010/08/12	P52-PWR-+1.5VP/+1.8VSP	Change PC152 to 330U	Change source
17.	2010/08/12	P52-PWR-+1.5VP/+1.8VSP	Change PL182 to SH00000GJ00	For shortage issue
18.	2010/08/12	P56-PWR_VGA_COREP	Add PQ604 TPCA8028	Add 1 low side MOS for VGA_CORE
19.	2010/08/12	P56-PWR_VGA_COREP	Add PR607 3.9k to 4.7k	set OCO to 39.62A
20.	2010/08/12	P56-PWR_VGA_COREP	Add PR622 20k	For non OPTIMUS enable
21.	2010/08/12	P55-PWR-CPU_CORE/GFX	Add PR576 0 Ohm	For disable GFX_CORE
22.	2010/09/08	P50-PWR-CHARGER	Change PU200 to ISL6251	Change source
23.	2010/09/08	P52-PWR-+1.5VP/+1.8VSP	Change PU150 to G5603	Change source
24.	2010/09/08	P53-PWR-+VCCSAP	Change PU450 to G5603	Change source
25.	2010/09/08	P54-PWR-+1.05VS_VCCP/+0.75VSP	Change PU400 to G5603	Change source
26.	2010/09/08	P53-PWR-+VCCSAP	Change OQ454 to MMST3904	Use low Vth transistor
27.	2010/09/08	P50-PWR-CHARGER	Add PQ217 2N7002W,PR249 10k	For precharge function
28.	2010/09/08	P50-PWR-CHARGER	Add PQ218 2N7002W,PR234 12.4k	For DC,QC CP setting
29.	2010/09/08	P53-PWR-+VCCSAP	Change PQ452 to A04712L	Use same part number
30.	2010/09/08	P53-PWR-+VCCSAP	Change PQ452 to A04712L	Use same part number
31.	2010/09/08	P53-PWR-+VCCSAP	Change PQ451 to A04466L	Use same part number
32.	2010/09/08	P50-PWR-CHARGER	Change PQ201,PQ202 to A04466L	Use same part number
33.	2010/09/08	P50-PWR-CHARGER	Change PQ201,PQ202 to A04466L	Use same part number
34.	2010/09/08	P50-PWR-CHARGER	Change PQ203,PQ207 to A04435L	Change source
35.	2010/09/08	P49-PWR_BATTERY CONN / OTP	Add PD5,PD6	For EMI request
36.	2010/09/08	P50-PWR-CHARGER	Change PR215 current sensor to 2512 size	Add current current senser rating
37.	2010/09/08	P55-PWR-CPU_CORE/GFX	Change PR551 from 3.83k to 3.65k	For CPU_CORE load line
38.	2010/09/08	P48-PWR_DCIN/VIN DECTOR	Add PR17 1k	For precharge function
39.	2010/09/08	Many page	Add 4.7 Ohm and 680pF	Add snubber
40.	2010/09/08	Many page	Add 2.2 Ohm	Add booster
41.	2010/09/08	P52-PWR-+1.5VP/+1.8VSP	Change PR181 0 to 150k,add PC185 0.1u	For VGA sequence
42.	2010/09/08	P53-PWR-+VCCSAP	Change Pr420 0 ohm to 0402 size	Cost down
43.	2010/09/08	P53-PWR-+VCCSAP	Change Pr410 0 ohm to 150k,add PC410 0.1u	For VGA sequence
44.	2010/09/08	P54-PWR-+1.05VS_VCCP/+0.75VSP	Change Pr463 0 ohm to 0402 size	Cost down
45.	2010/09/08	P49-PWR_BATTERY CONN / OTP	Add PR29 100k,PR22 1.02k,PR27 4.99k,PR28 4.53k	For adapter protect function
46.	2010/09/08	P52-PWR-+1.5VP/+1.8VSP	Change PR151 4.7k to 7.5k	For UMA 1.5V OCP
47.	2010/09/08	Many page	Add 10u 1206	For EMI ISN request
48.	2010/09/08	P50-PWR-CHARGER	Add PL201	For EMI ISN request
49.	2010/09/08	P50-PWR-CHARGER	Change VGA IC solution(many component)	For cost down
50.	2010/09/08	P53-PWR-+VCCSAP	Change PR455 2.2 to 0	remove booster

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Power PIR		
				Size	Document Number	Rev
					PHQAA LA-6831P M/B	0.1
Date:				Thursday, October 07, 2010	Sheet	57 of 58